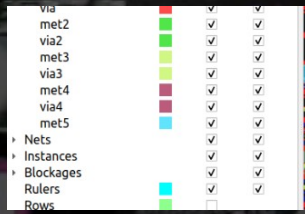
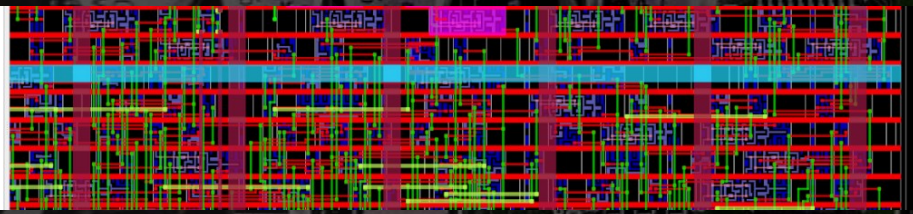
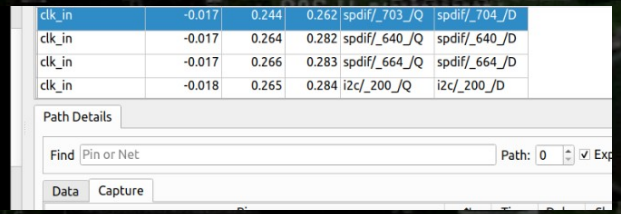
Open Source chip Design
Tiny Tapeout intro

BVM Engineering College
Webinar I
September 30 - 2026







IC WORKS
Jørgen Kragh Jakobsen

Plan:

2:00 PM	Intro to the Open-Source Chip Design Eco system
2:25 PM	Intro to Tiny Tapeout
2:45 PM	QnA + 5 min break
2:55 PM	Open Source tools you can start with
3:10 PM	QnA + Next session

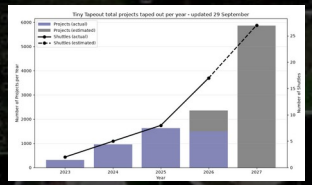

YosysHQ
Surfer
24h
XILINX®
SPARTAN®
Why?
President Trump & Xi
Let's meet in Hong Kong

Current state of Open-Source Chip Design

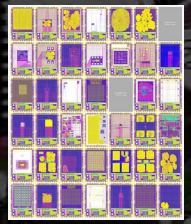
Open MPW Shuttle Program
efabless
Sponsored by Google

Google + GLOBAL FOUNDRIES
FOSS 180nm Production PDK
github.com/google/gf180mcu-pdk

csem EPFL ETH zürich ihp

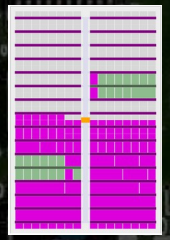


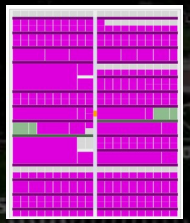
24h OpenROAD efabless.com

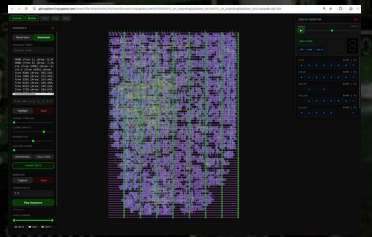


TINY TAPEOUT









FSiC2019
Free Silicon Conference

FSiC2022
Free Silicon Conference
July 7-9, Paris, Sorbonne Université
FSI

FSI
Free Silicon Conference 2023
FSiC2023
Free Silicon Conference
Genre: Free software and free hardware development conference
Location(s): Paris, Sorbonne Université
Country: France
Website: wiki.f-si.org/index.php/FSiC2023@
July 10,11,12 2023

FSiC2024
Free Silicon Conference

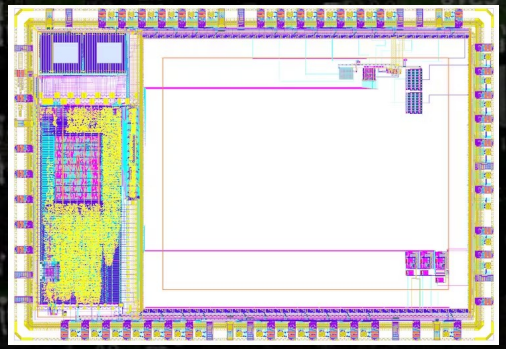
Free Silicon Conference 2025
FSiC2025
Free Silicon Conference

Free Silicon Conference 2026
FSiC2026
Free Silicon Conference

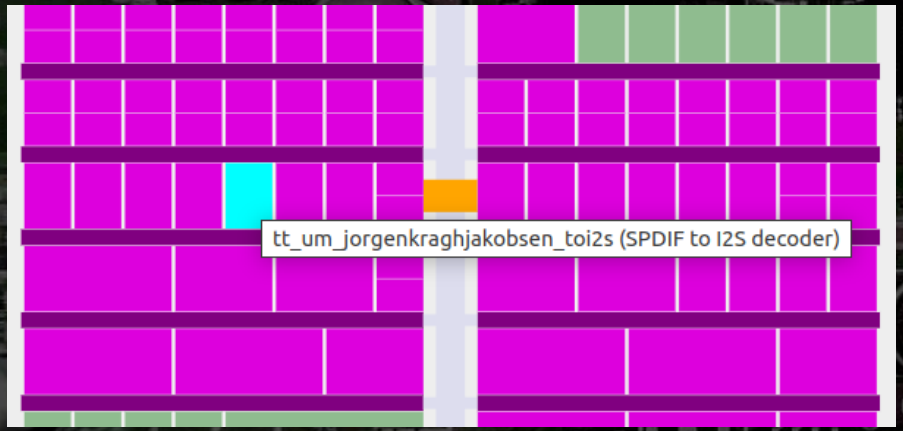
Tiny Tapeout







My TT06 submission

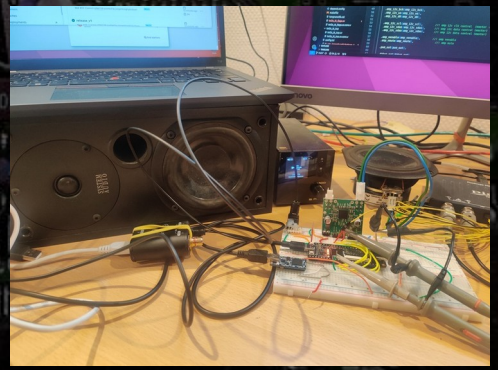


README Apache-2.0 license

gds passing docs passing test failing

SPDIF to I2S - from blinky light to sweet audio

- Take single input serial bitstream SPDIF audio source and convert to standard I2S



https://github.com/jorgenkraghjakobsen/tt06-toi2s

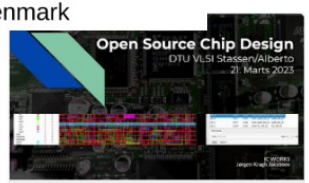
LAST 5 Years

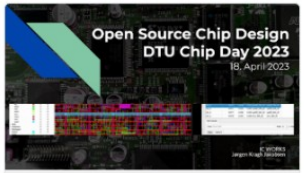
Open Source IC design

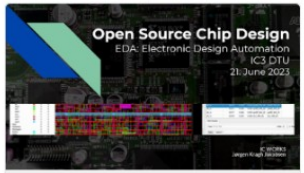
Jørgen Kragh Jakobsen
Bornhack 2021
Denmark

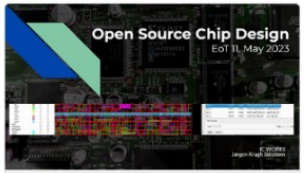














AARHUS UNIVERSITET



Free Silicon Conference 2023

Free Silicon Conference 2024

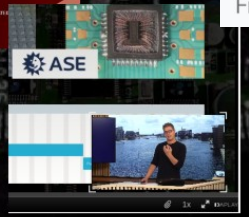
FSiC2024

Free Silicon Conference 2026

FSiC2026

Free Silicon Conference

nlnet FOUNDATION

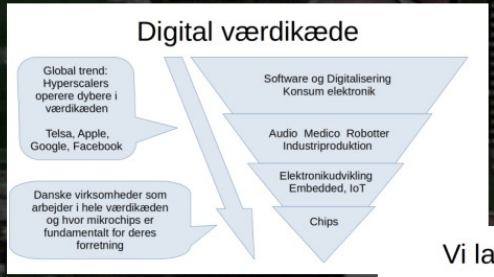


SDU

IoT, FPGA, Arch
Consulting
Bread and butter



Questions to Ministers



Vi laver masser af chips i DK

- Ingeniører som har specialiseret sig i chip design
- Dominere områder: Audio, Netværk og Wireless
- Komplette uddannelsestilbud på området (DTU og AU)
- Tiltrækker globale spillere
  - Intel, Nvidia, Infineon, Microchip
- Mange chip startups
  - Fødekæde af innovation





Spørgsmål 127

Vil ministeren i samarbejde med erhvervsministeren og ministeren for forskning og uddannelse oplyse, hvilke tanker regeringen gør sig i forhold til at udarbejde en strategi for at sikre, at der fortsat er et levende chipudviklingsmiljø i Danmark?

Til: digitaliseringsminister Marie Bjerre (V)
Dato: 20-09-2023
Status: Ikke besvaret

Spørgsmål 128

Mener ministeren, at der er behov for en dansk strategi, der understøtter ambitionerne i EU Chip Act, og hvilke initiativer vil ministeren i bekræftende fald tage for at udvikle en sådan?

Til: digitaliseringsminister Marie Bjerre (V)
Dato: 20-09-2023
Status: Ikke besvaret

We got the money
But no plan

Aftale om fordeling af forskningsreserve mv. i 2024

Regeringen og aftalepartierne er enige om at fordele 3.814,5 mio. kr. til initiativer i finansloven for 2024, *jf. tabel 1 nedenfor*.

2.7. Forskning i halvledere, micro- og nanochips

Aftalepartierne er enige om at afsætte 30,0 mio. kr. til at understøtte dansk deltagelse i europæiske forsknings- og udviklingsinitiativer inden for halvledere, micro- og nanochips, herunder særligt etablering af et nationalt kompetencecenter. Mikrochips er grundstenen i den digitale omstilling af vores samfund og indgår i en lang række af produkter. EU har afsat 24,6 mia. kr. til at øge europæisk forskning og udvikling inden for mikrochipområdet og øge virksomheders kapacitet i forhold til at producere mikrochips på kontinentet. Danmark kan med en øget national bevilling inden for mikrochips bane vejen for at underbygge danske styrkepositioner på området – og samtidig øge muligheden for hjemtag af europæiske midler.

Midlerne afsættes til medfinansiering af nationalt kompetencecenter 2024-2027. Midlerne udmøntes af Uddannelses- og Forskningsministeriet. Evt. uforbrugte midler kan udmøntes gennem det europæiske partnerskab Chips JU under Danmarks Innovationsfond.


DIGITAL

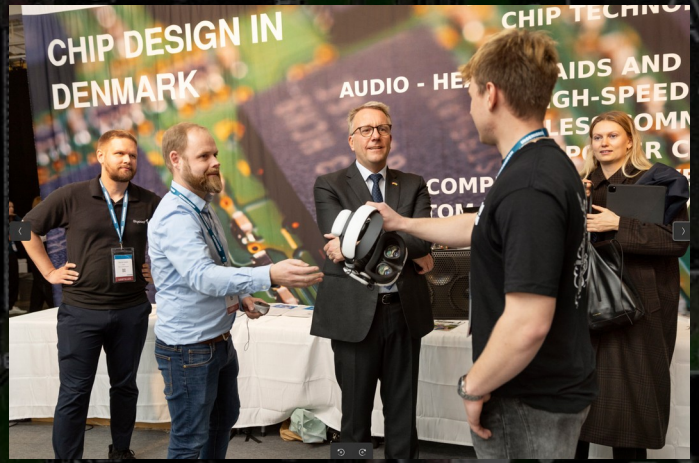

DIGITAL TECH
SUMMIT


DIGITAL TECH

Vilde teknologier Aarhus 2024









India Semiconductor Mission 2.0

A Major Push in Budget 2026 towards Semiconductor Self-Reliance

Posted On: 07 FEB 2026 1:13PM by PIB Delhi

Key Takeaways

- Union Budget 2026–27 allocates ₹1,000 crore for **India Semiconductor Mission (ISM) 2.0.**
- As of December 2025, **10 ISM projects worth ₹1.60 lakh crore** approved across six states.
- India's semiconductor market projected to reach **$100–110 billion by 2030.**



kunal ghosh (vlsisystemdesign.com) • 1st

Co-Founder at VLSI System Design (VSD)

Visit my website

9mo •

Two back-to-back tech podcasts in a row - diving deep into **#OpenSource** **#EDA**, **#RISCV**, and the **India Semiconductor Mission**. Exciting conversations, inspiring people, and a future being built in real time. Full details coming soon. Stay tuned!





30 year in Chip Design

Analog/Digital Chip design

Startups, big corps

Written lots of software, flows and web services to get the job done

Work smarter - not harder





NOKIA

oticon PEOPLE FIRST

MERUS AUDIO

infineon

IC WORKS

simplewire

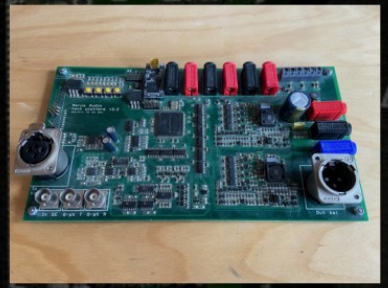
s(ONIC EDG)e

ERICSSON

SILICIDE

nlnet FOUNDATION

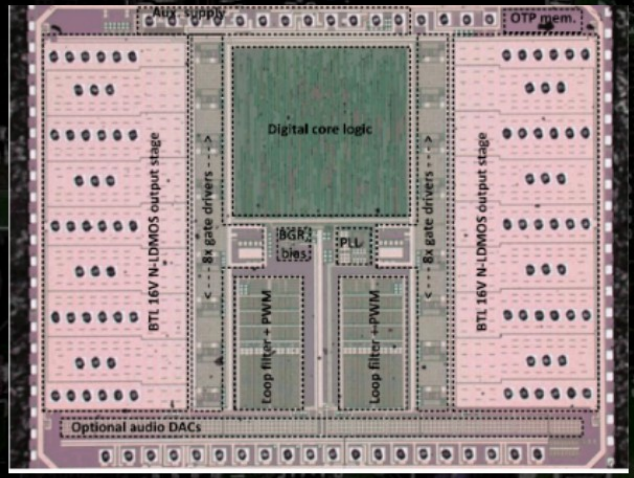
Chip design is super complex most cases a hidden industry



Analog and digital circuit design, auto and manual layout

IO connected through a complex padring
2000V ESD

Top level mixed mode simulation at different model levels.
Startup voltage ramp up



Test and reliability devices spread 30-40% over temp, voltage and process

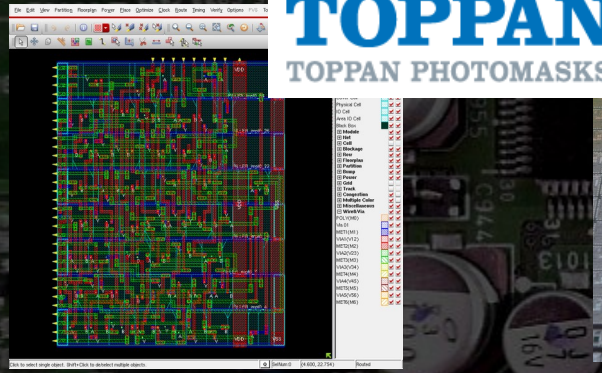
Design rule check
LVS: Sch vs Layout
1-5 hour jobs with expensive EDA software



2x80W audio amp 3x4mm2
180nm 30V process

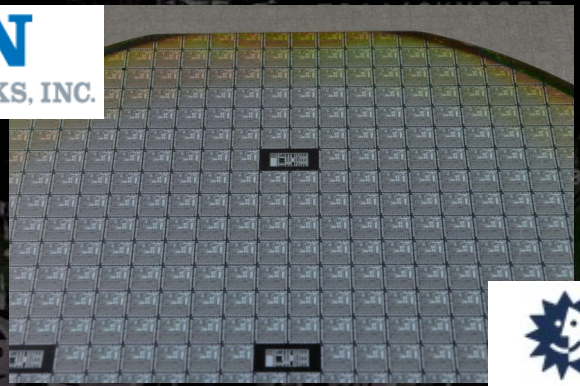
Infineon	Infineon	429	$ 5.2	1

Chip development as fabless designer

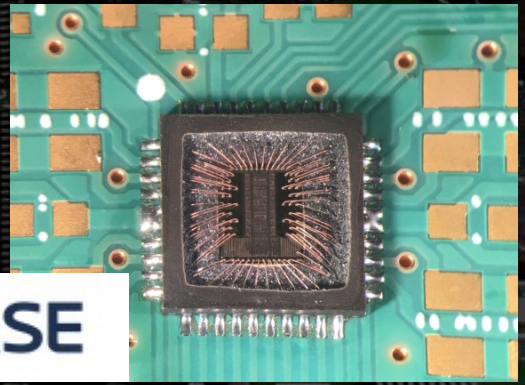


TOPPAN

TOPPAN PHOTOMASKS, INC.



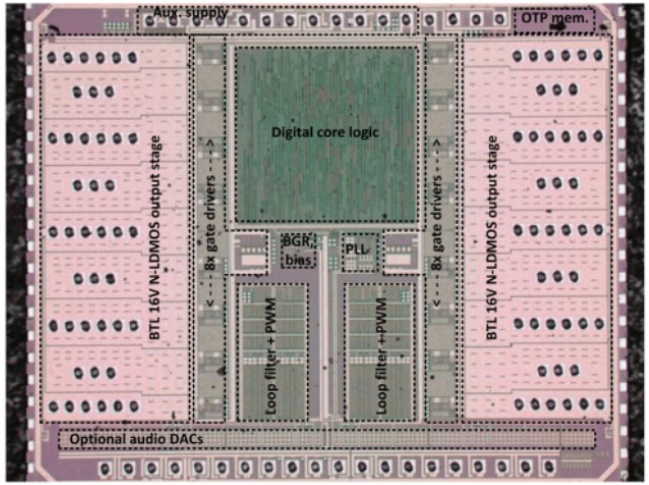
ASE





Full custom chip design

Merus first generation



2 x 80W 4xSE/2.1/2BTL/PBTL

3/5-level switching

16V NMOS stacked output stage

Analog/Digitial input (4 DAC's)

50 uVrms noise level ~100 dB THD+N aweighted

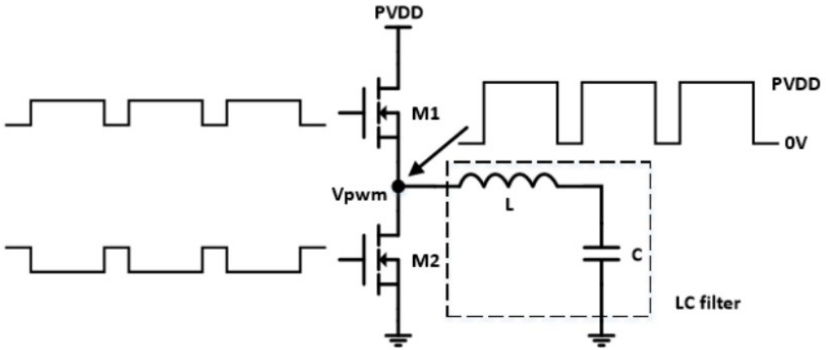
Build in self test / OTP production test and device tracking

180nm Dongbu Hightek Sells in millions

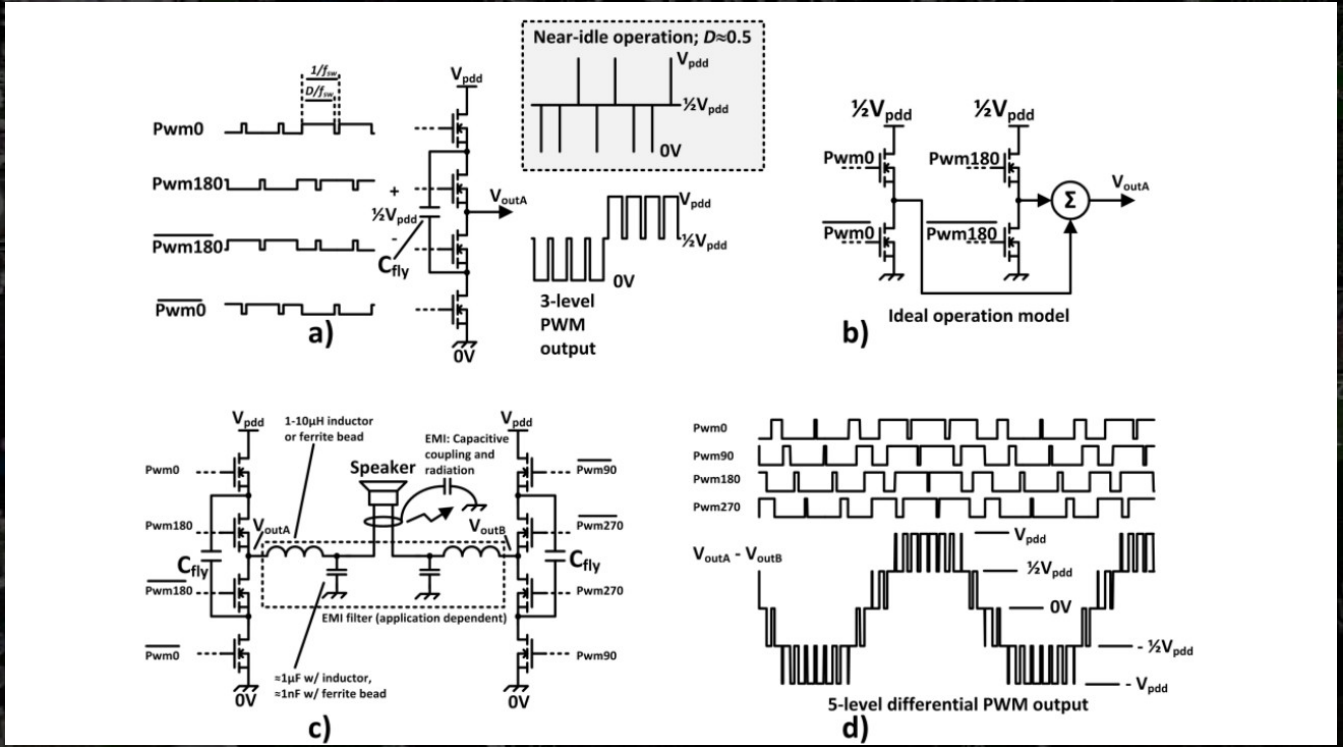
Full custom chip design

Audio Class D amps

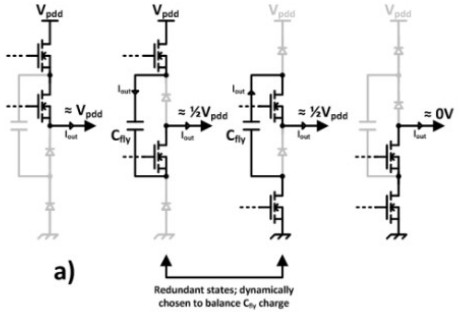
Traditional class D (20 year old tech)
– Large Idle loss – even at moderate volume
– Effective only at max power
– EMC issues
– Complex descrete rail tracking

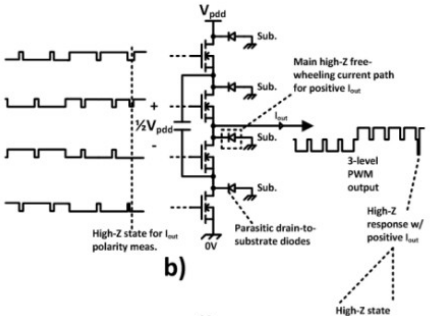


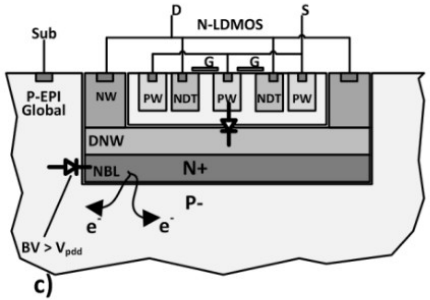
Full custom chip design

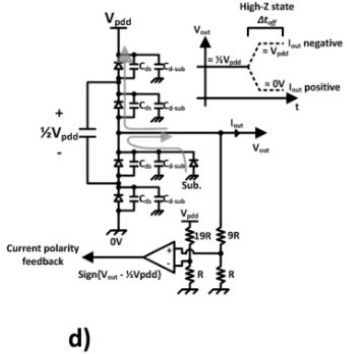


Full custom chip design







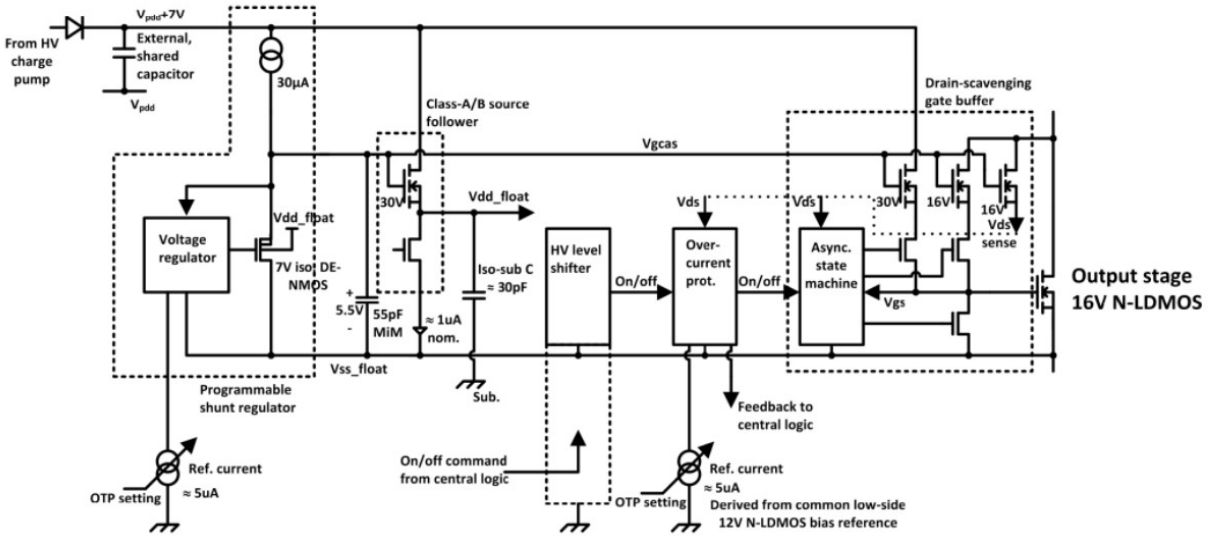


Flycaps transistor stack to generate PVDD/2

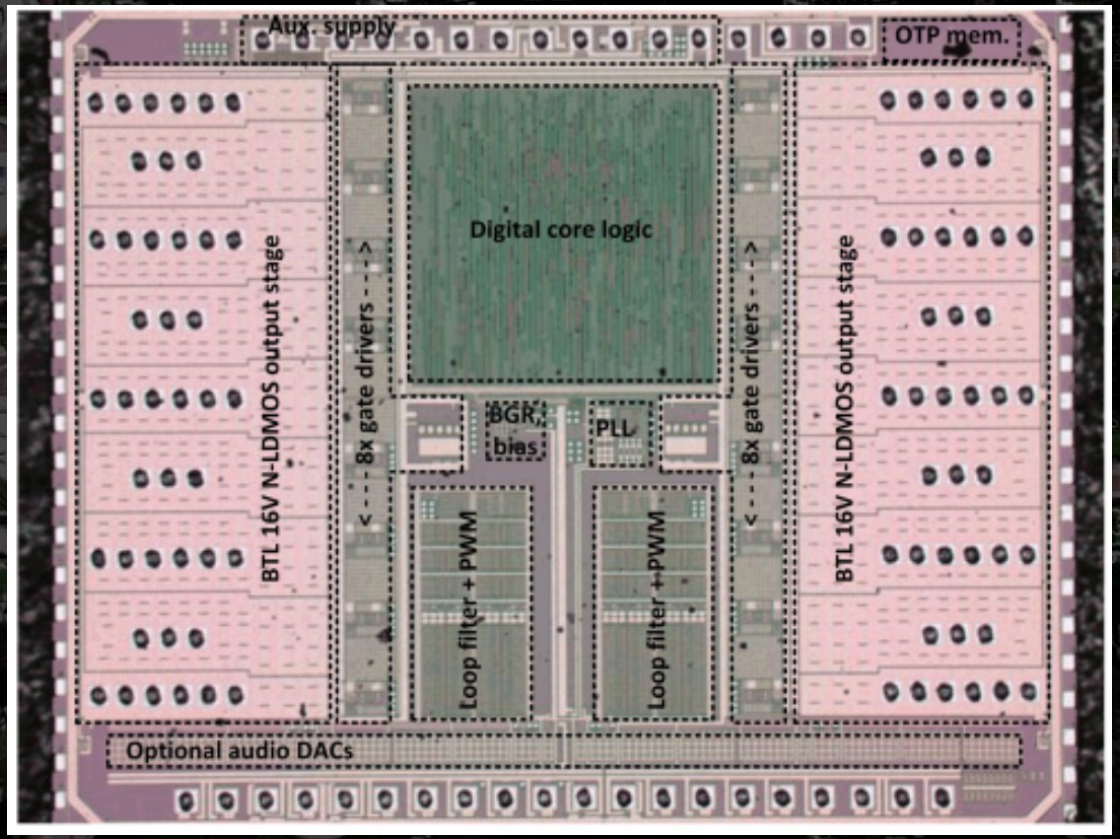
Tripple well BCD process

Full custom chip design

Patent: Turning on/off a transistor

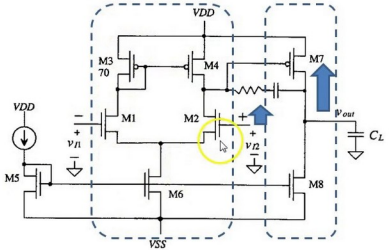


Full custom chip design



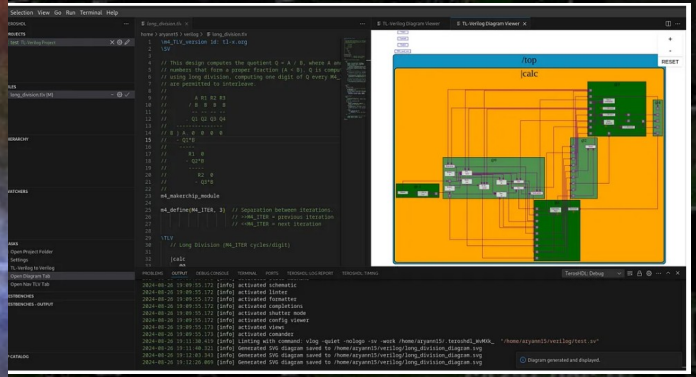
Analog vs Digital chip design

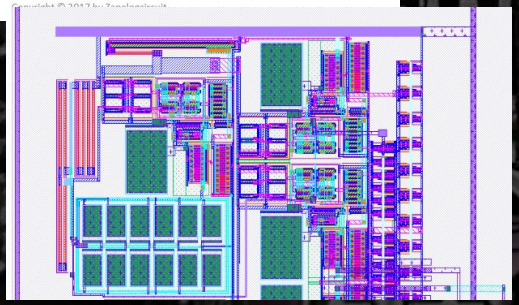
Single Stage Amp+CS

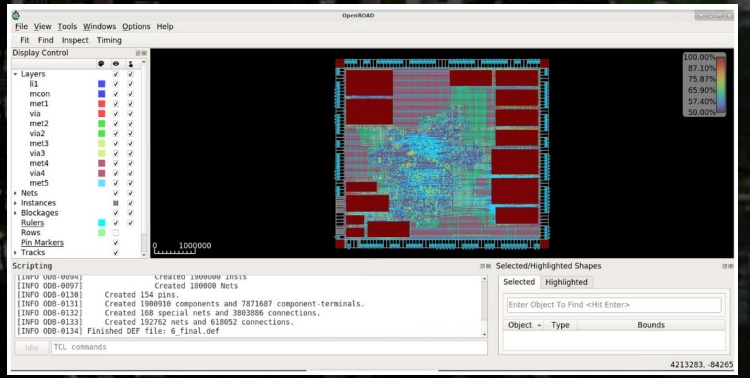


- 1st stage gain is about a hundred. Not enough for many applications. Add CS stage to increase gain to 60dB+.
- Gain = gm2*ro4//ro2 (diff) * gm7 * ro7//ro8 (CS)



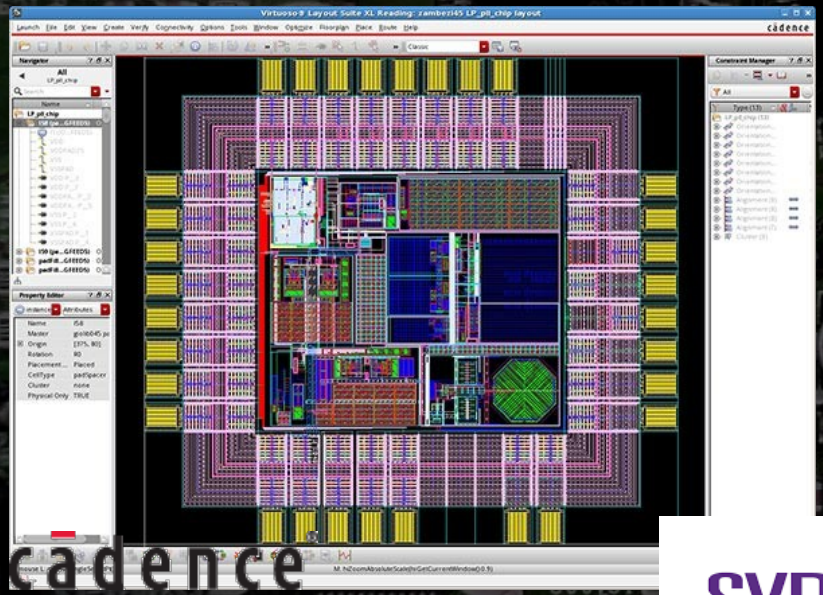


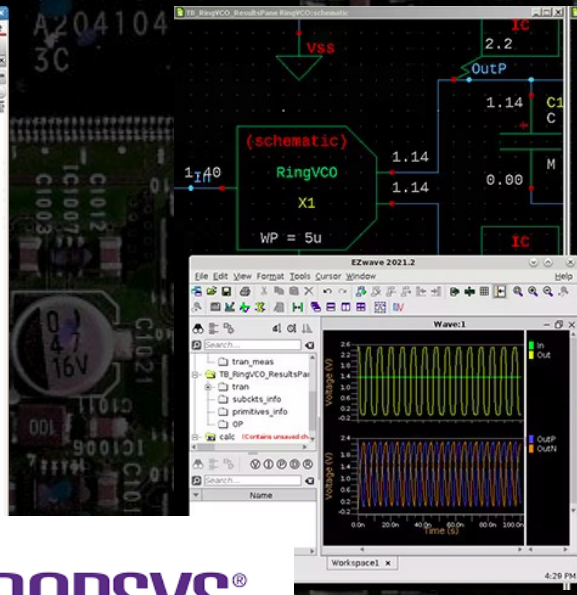


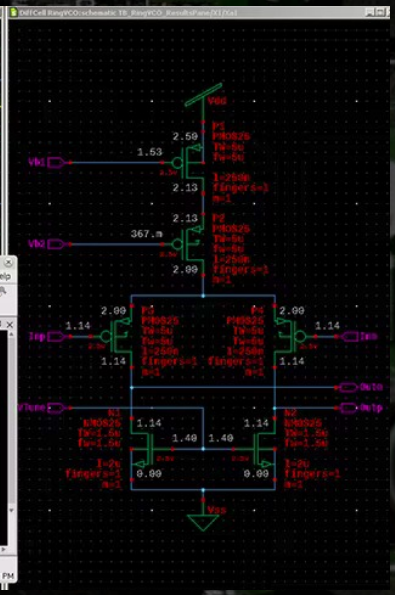


Chip Design Tools
Industry standard

SIEMENS
Mentor Graphics







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STD logic Opamp's LDO's	MCU's ASIC's	CPU's GPU's TPU's
Analog/Digital 600 - 90 nm Old nodes	Analog/Digital 90 - 45 nm Mature nodes	Digital 22-5 nm Leading edge
Dirt cheap	Cheap	Expensive

Leading / Lagging edge

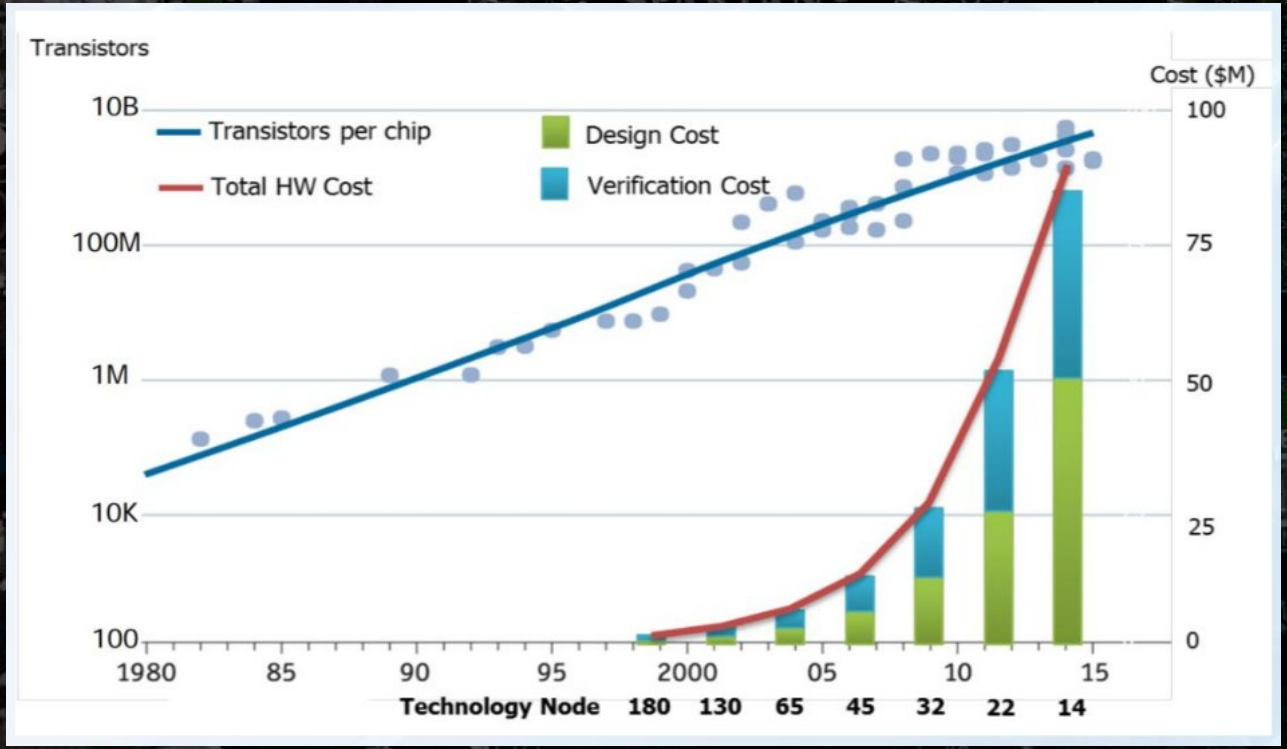


Image credit: A. Olofsson, keynode, Intl. Symp. on Physical Design, March 2018

Moores Law died 10 years ago

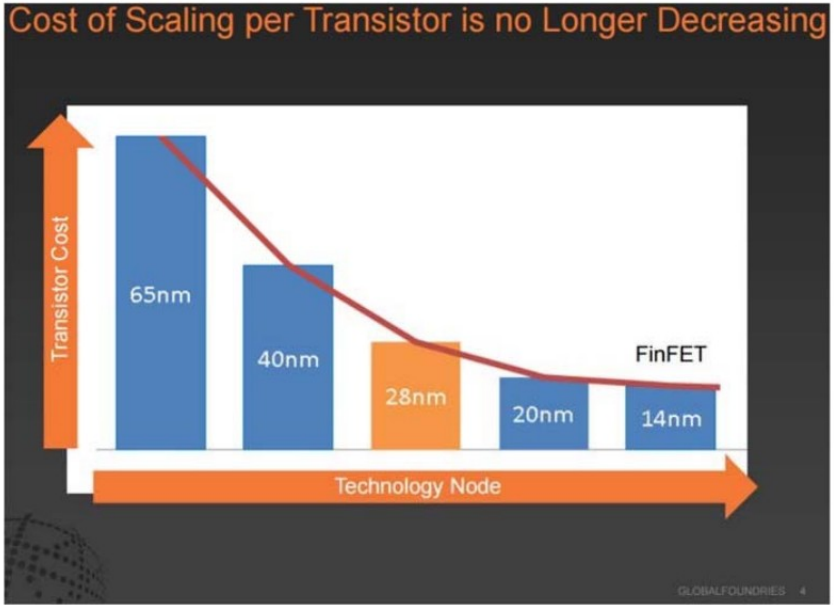
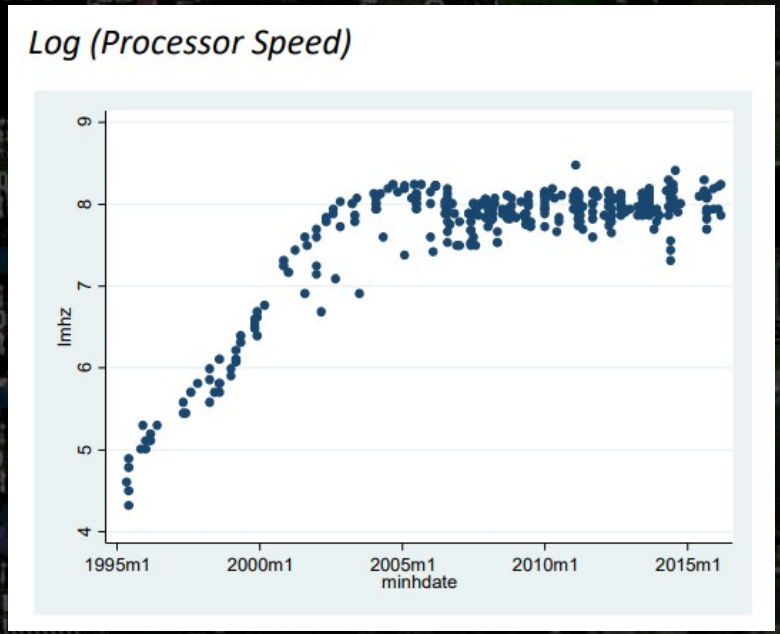


Figure 5. Global Foundries' Transistor Manufacturing Cost at Recent Technology Nodes
Source: McCann (2015).



Chip industry crisis

Lag of innovation

Major lag of chip designers

EE declines - CS increase - SW exploded

Tools cost set set by leading edge - Very expensive

Marked monopoly on tools

Access to PDKs fenced by NDA’s

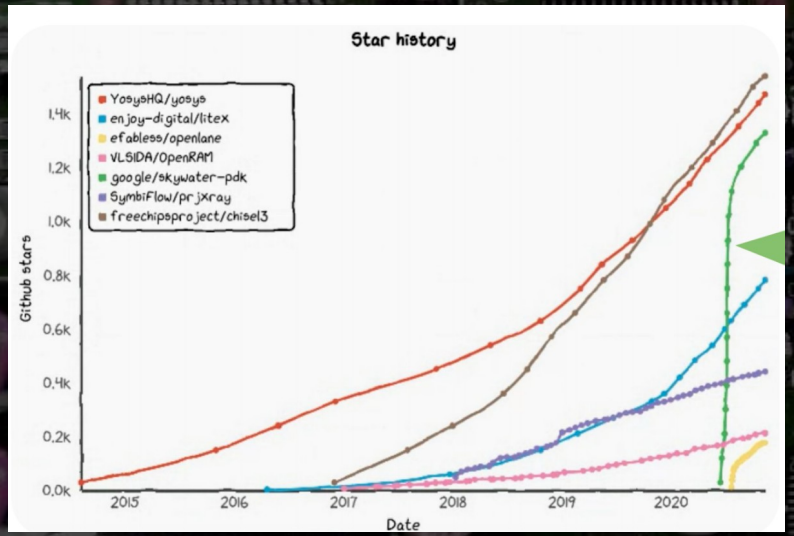
Hey Google help us

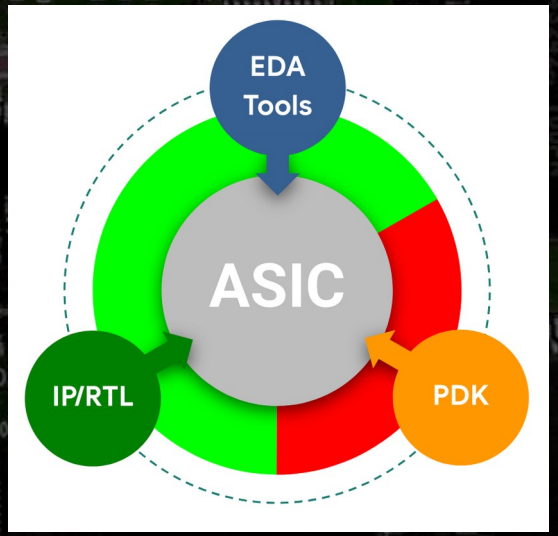
http://bit.ly/vsdopen22-goog

Google + skywater TECHNOLOGY

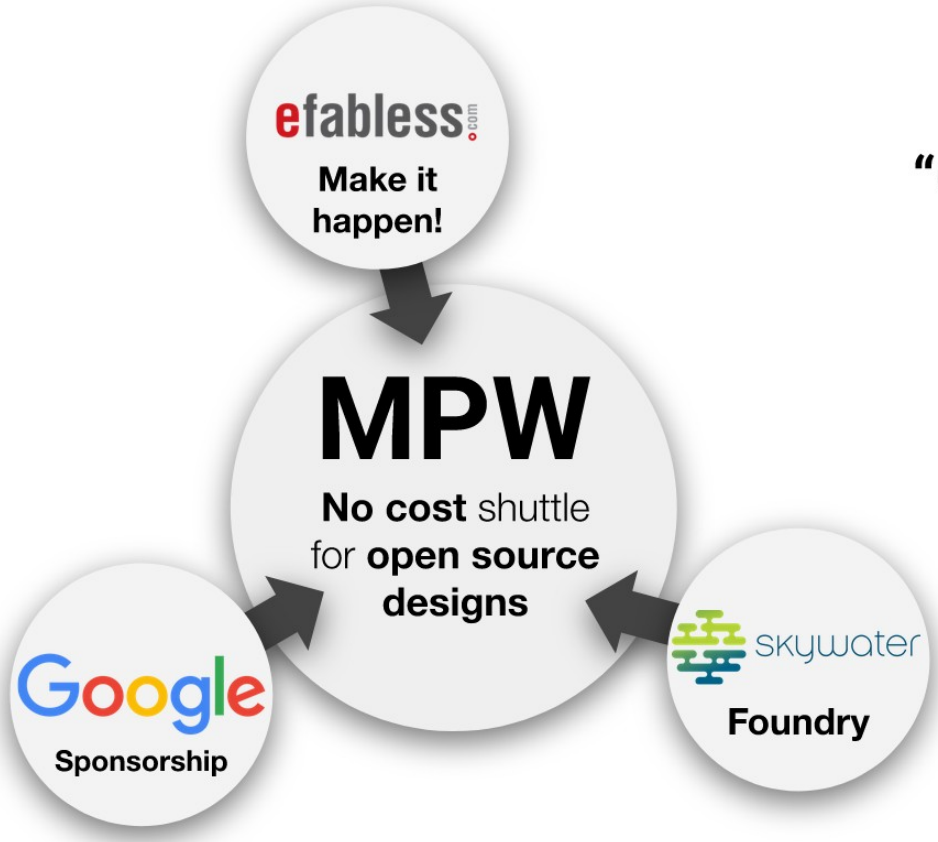
FOSS 130nm Production PDK

github.com/google/skywater-pdk





Silicon Realization Program



The SKY130

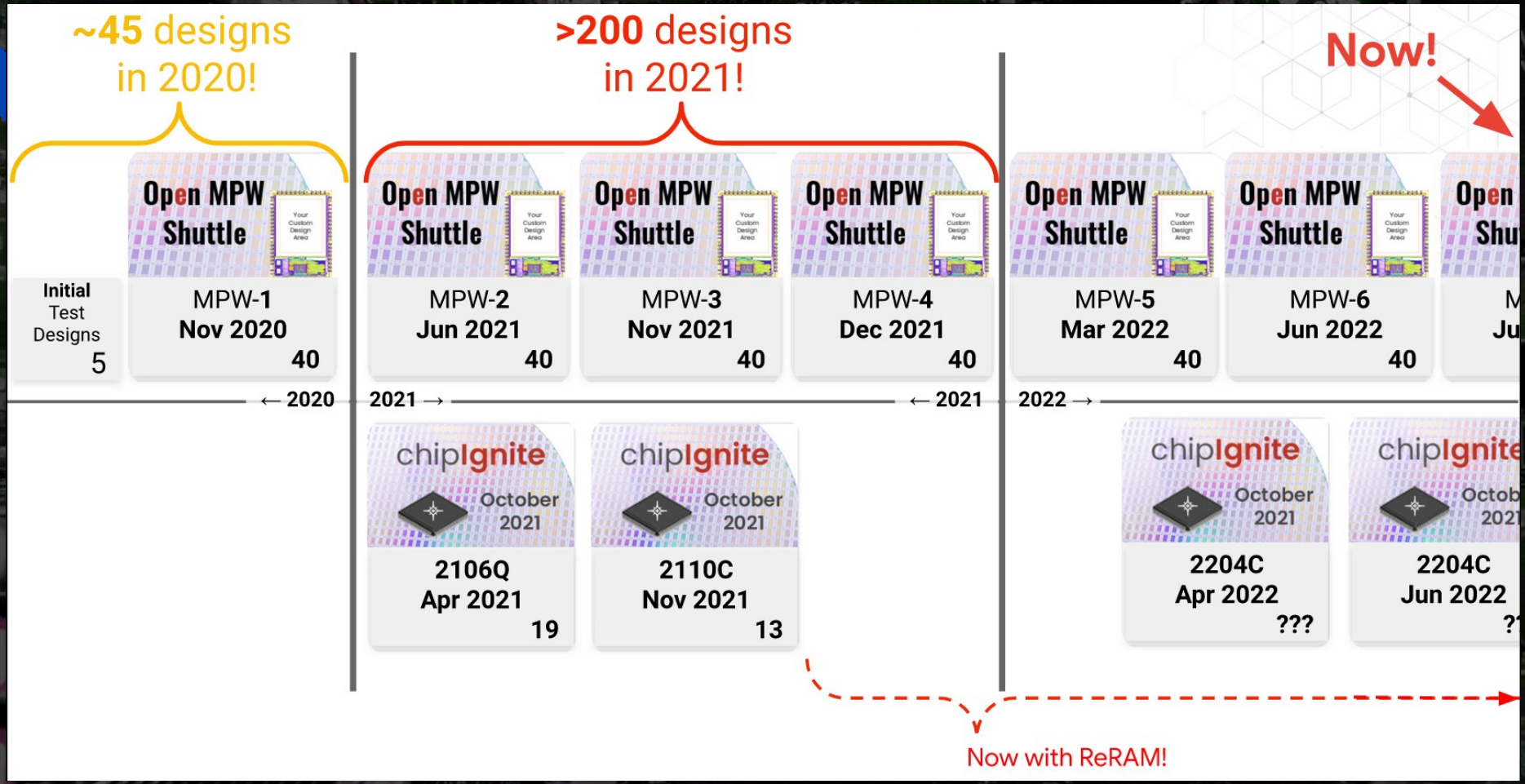
“Open MPW Shuttle Program”

is **managed** by efabless,

funded by Google and

manufactured by SkyWater.

bit.ly/vsdopen22-goog


~45 designs in 2020!
>200 designs in 2021!
Now!
Open MPW Shuttle
Initial Test Designs 5
MPW-1 Nov 2020 40
MPW-2 Jun 2021 40
MPW-3 Nov 2021 40
MPW-4 Dec 2021 40
MPW-5 Mar 2022 40
MPW-6 Jun 2022 40
← 2020
2021 →
← 2021
2022 →
chipIgnite October 2021
2106Q Apr 2021 19
2110C Nov 2021 13
2204C Apr 2022 ???
2204C Jun 2022
Now with ReRAM!

MPW - Multi Project Wafer

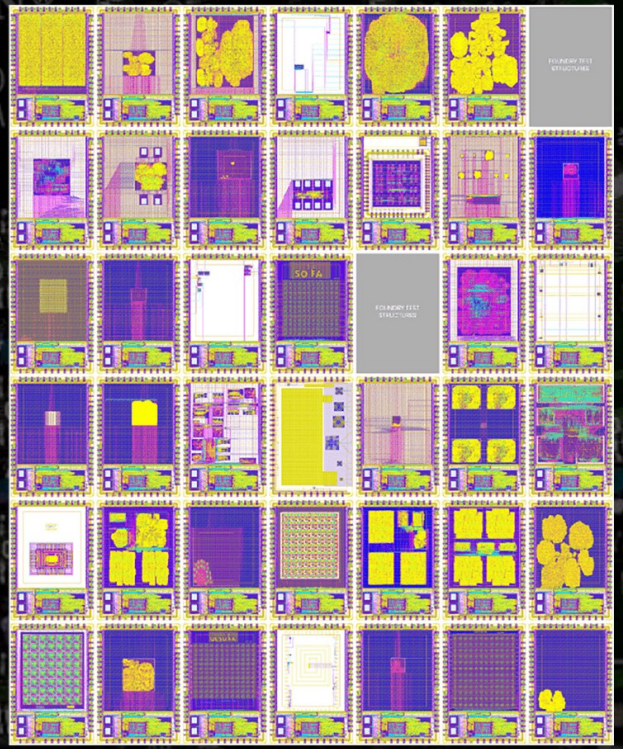
6x7 chips stepped over the full wafer

Reducing prototype cost from

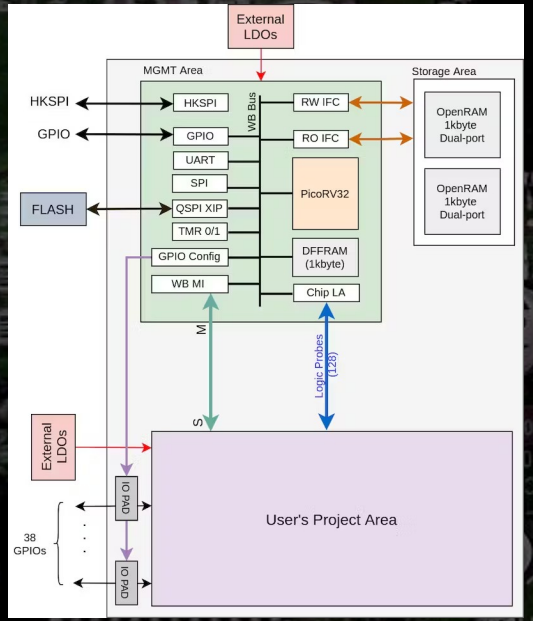
100k USD -> 20k USD

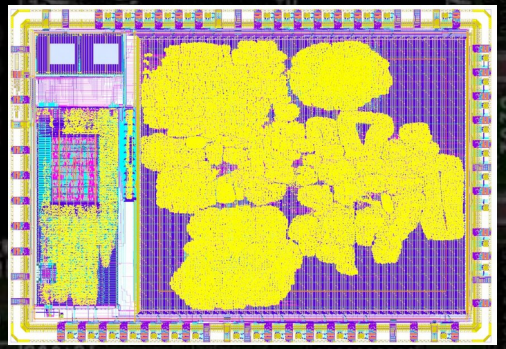
Normally you never see other chips that

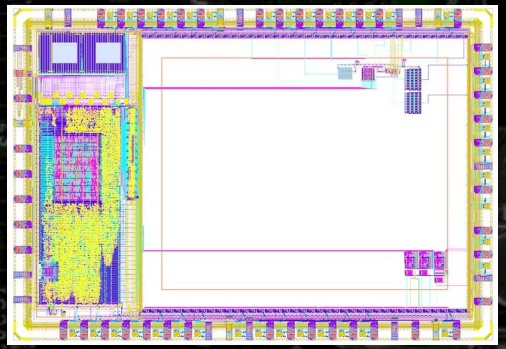
you share MPW with

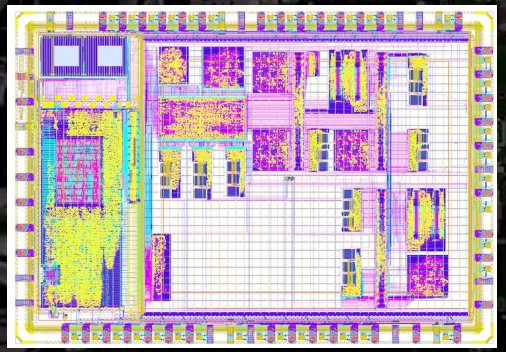


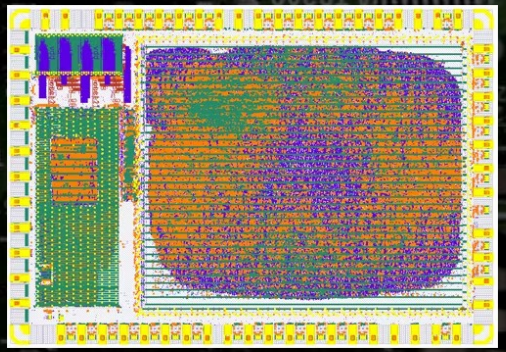
What kind of chips











Making things easier?

@proppy
Johan Euphrosine
<proppy@google.com>



Packaging

conda-eda

github.com/hdl/conda-eda



Computational documents

Jupyter Notebook

github.com/chipsalliance/silicon-notebooks/



Cloud-friendly tooling

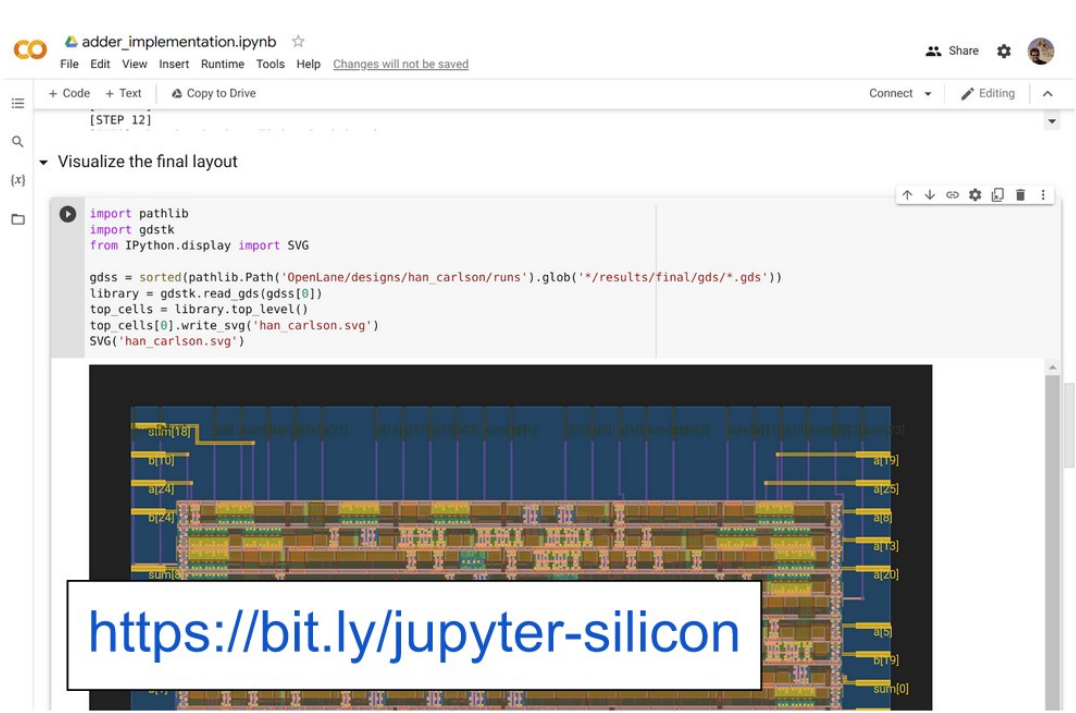
RAD Lab module for Silicon Research

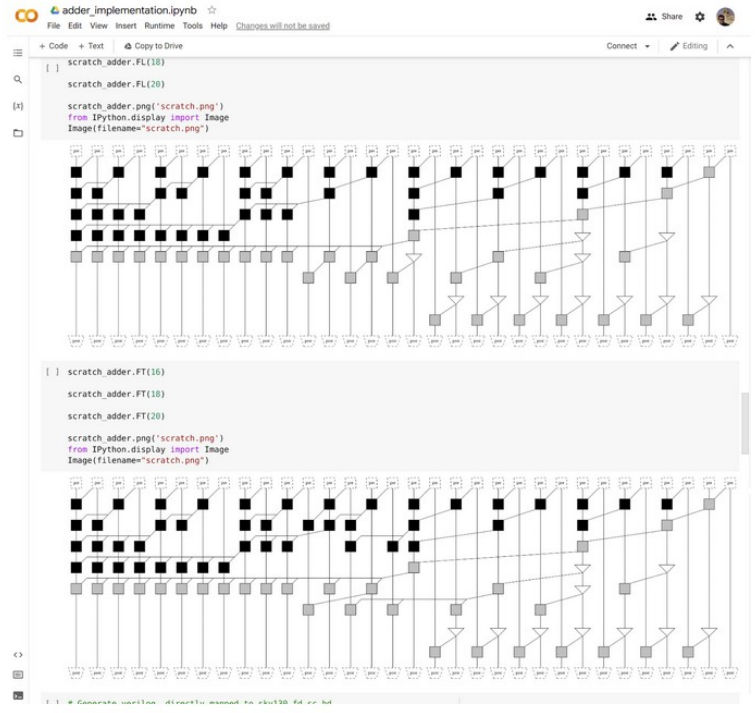
github.com/proppy/rad-lab

Google Cloud Platform *makes things easier!*

Adders in Jupyter Notebooks (Google Colab)

Just share an URL!





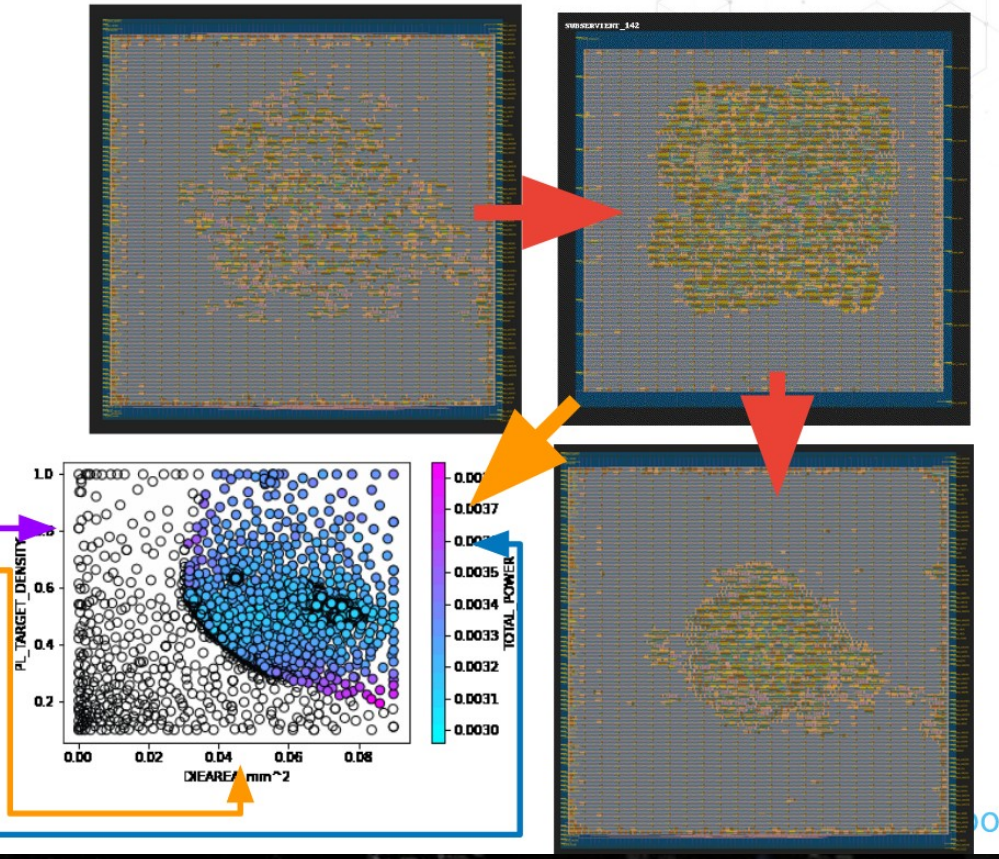
Google Cloud Platform *makes things easier!*

Vertex AI Tuning

```python
from google.cloud import aiplatform

hpt_job = aiplatform.HyperparameterTuningJob(
    display_name='inverter-tuning-job',
    custom_job=custom_job,
    metric_spec=metric_spec,
    parameter_spec=parameter_spec,
    max_trial_count=200,
    parallel_trial_count=10,
    max_failed_trial_count=200)

hpt_job.run()
```

```python
from google.cloud.aiplatform import hyperparameter_tuning as hpt

parameter_spec = {
    'target_density': hpt.DoubleParameterSpec(min=10, max=100, scale='log'),
    'die_width': hpt.DoubleParameterSpec(min=10, max=300, scale='linear'),
}

metric_spec={'total_power': 'minimize'}
```

https://bit.ly/jupyter-silicon



IEEE Solid State Circuits Society

- 2021 PICO Chipathon Contest
  - **61 design proposals**
  - 18 selected
  - 11 taped out
- IEEE & SSCS Student memberships offered to all participants
- New SSCS Student Branch Chapters started by team leads
- 2022's Edition is on-going with overall a better quality and ambitious projects


Boris Murmann
Stanford
USA


Thomas Brandtner
Infineon
Austria


Francisco Brito Filho
Fed. Univ. Semiarido
Brazil


J. Dhurga Devi
Anna Univ.
India


Jaeduk Han
Hanyang Univ.
Korea


Chiraag Juvekar
Analog Devices
USA


Rana Muhammad
FAST National
Univ. Pakistan

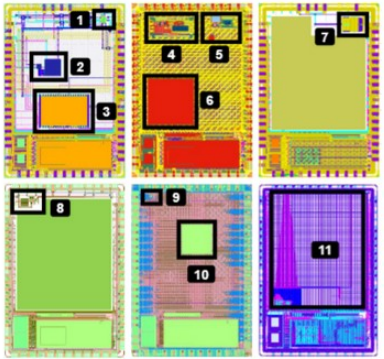

Harald Pretl
Kepler Univ., Linz
Austria


Priyanka Raina
Stanford
USA


Mehdi Saligane
Univ. Michigan
USA


Mirjana Videnovic-Misic
Silicon Austria Labs
Austria

New Open-Source Ecosystem Technical Committee



	Function	Team	Chip URL
1	5G bidirectional amplifier	Pakistan3 (FAST National University)	https://efabless.com/projects/560
2	Wireless power transfer unit	Pakistan2 (FAST National University)	
3	Variable precision fused multiply-add unit	Pakistan1 (FAST National University)	
4	Oscillator-based LVDT readout	India2 (Anna University)	https://efabless.com/projects/474
5	Temperature sensor	India1 (Anna University)	
6	GPS baseband engine	India3 (Anna University)	
7	Ultra-low-power analog front-end for bio signals	Brazil2 (U. Federal de Santa Catarina)	https://efabless.com/projects/476
8	TIA for quantum photonics interface	USA4 (University of Virginia)	https://efabless.com/projects/470
9	Bandgap reference	Egypt (Cairo University)	https://efabless.com/projects/473
10	Neural network for sleep apnea detection	USA2 (University of Missouri)	
11	SONAR processing unit	Chile (University of the Bio-Bio)	https://efabless.com/projects/540

Open-Source Design Notebook Competition & Travel Grant Award

- Inspired by existing programs of SSCS and CAS
  - www.ieee-cicc.org/travel-grants/student-travel-grant-awards/
  - students.ieee.org/funding-opportunity/2021-cass-student-travel-awards/
  - Award around $2.5k for travel and accommodation may make sense, plus separate dollar amount for conference registration
- Multiple rounds per year
  (essentially always an open call)
- Accessible and flexible for people to participate; casts a wide net to maximize participation

Conference	Date
ISSCC	Feb 18
CICC	Apr 20
ISCAS	May 28
VLSI	June 12
ESSCIRC	Sep 20
A-SSCC	Nov 6

Open Source Chip Design in Danmark

DTU Compute
3.5K followers
2mo •

DTU Chip Day! The very first of its kind at **DTU** - Technical University of Denmark - for students and industry. 162 participants! An afternoon with industry presentations, some info on **chip** design and verification education, and plenty...



DTU

Uddannelse Efteruddannelse Forskning Innovation Samarbejde Om DTU Nyheder



Første DTU-mikrochip bygget med open source-værktøj

ELEKTROTEKNOLOGI INFORMATIONSTEKNOLOGI MATEMATIK

FREDAG 06 MAJ 22 af Hanne Kokkegård

12 studerende har designet en chip med gratis software, og den bliver produceret i USA uden omkostninger gennem et Google-initiativ.

Der er altid en festlig stemning på DTU, når de studerende afslutter et 13 uger langt semester. Dette forår skriver 12 studerende samtidig historie på DTU Compute. Siden februar har de fulgt et specialkursus i chipdesign.

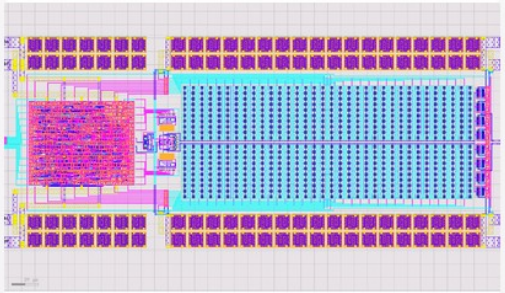
Kurset er historisk af flere grunde: Det er første gang, at DTU underviser i chipdesign som et semester-fag for bachelor- og kandidatstuderende. Det er også første gang, at man anvender open source-værktøjer til at designe mikrochippen med. Tilmed bliver chippen produceret gratis i USA i



KONTAKT

Martin Schoeberl
Professor
DTU Compute
45 25 37 43
masca@dtu.dk

Open Source Chip Design from Denmark

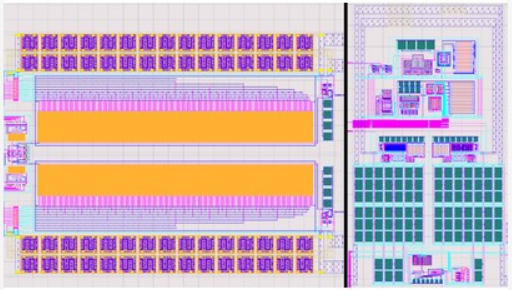


8-bit SAR-ADC... public

Christoph Weiser

This is a Analog to Digital Converter based on the popular SAR architecture. It has 8-bit...

MPW-3 SKY130A 741

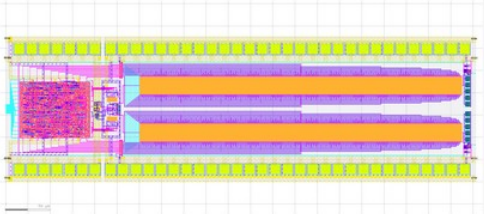


SAR-ADC and... public

Christoph Weiser

This submission consists of a updated 8-bit SAR-ADC, basic analog support circuitry, such as...

MPW-4 SKY130A 448



10b ADC and... public

Christoph Weiser

This submission features: 10b SAR-ADC, Bandgap reference, Testbuffer, Clock generator, LDO,...

MPW-6 SKY130A 0

https://platform.efabless.com/projects/shuttle_1

25 years of Open-Source - software

1998: Re-branded from software freedom

1999: Open source definition licenses and standards

2001: “Linux is a cancer” – Microsoft

2003: SCO sues IBM over Linux

2005: UNIX now open source

2007: Java now open source

2008: Top level management ack benefits of open source

25 years of Open-Source SW

2008: Most open source is hidden infrastructure

2011: Open source hits web develop business

2013: Open source powering cloud/container revolution

2015: “Microsoft love Linux” – Microsoft

2016: Windows Subsystem for Linux 1 (WSL1) released

2017: Open source tools and frameworks dominate new software

2019: Windows Subsystem for Linxu 2 (WSL2) released

2020: Windows brings Linux GUI apps to Windows 10

Source: Simon Phipps OSI

Next 10 year in Open-Source Hardware

Exponential development 20 year -> 10 year

More Open Source PDKs and abstractions

Start to see innovation in our EDA tools

More higher level system languages in digital

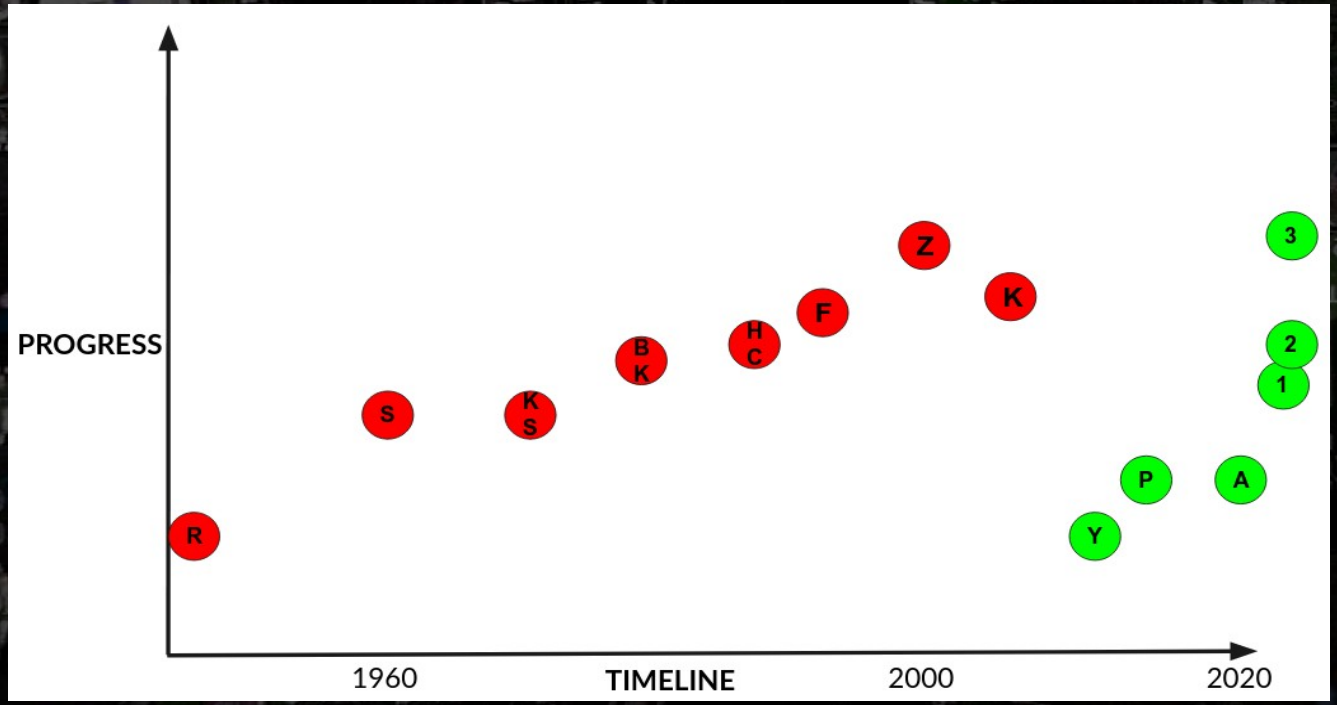
Analog layout generators and optimizers



Adders in Yosys

FOM for hardware adders in VLSI reported in papers(red) - Open source tools (green)

https://github.com/mattvenn/instrumented_adder



THE LINUX FOUNDATION



F4PGA
A CHIPS ALLIANCE WORKGROUP

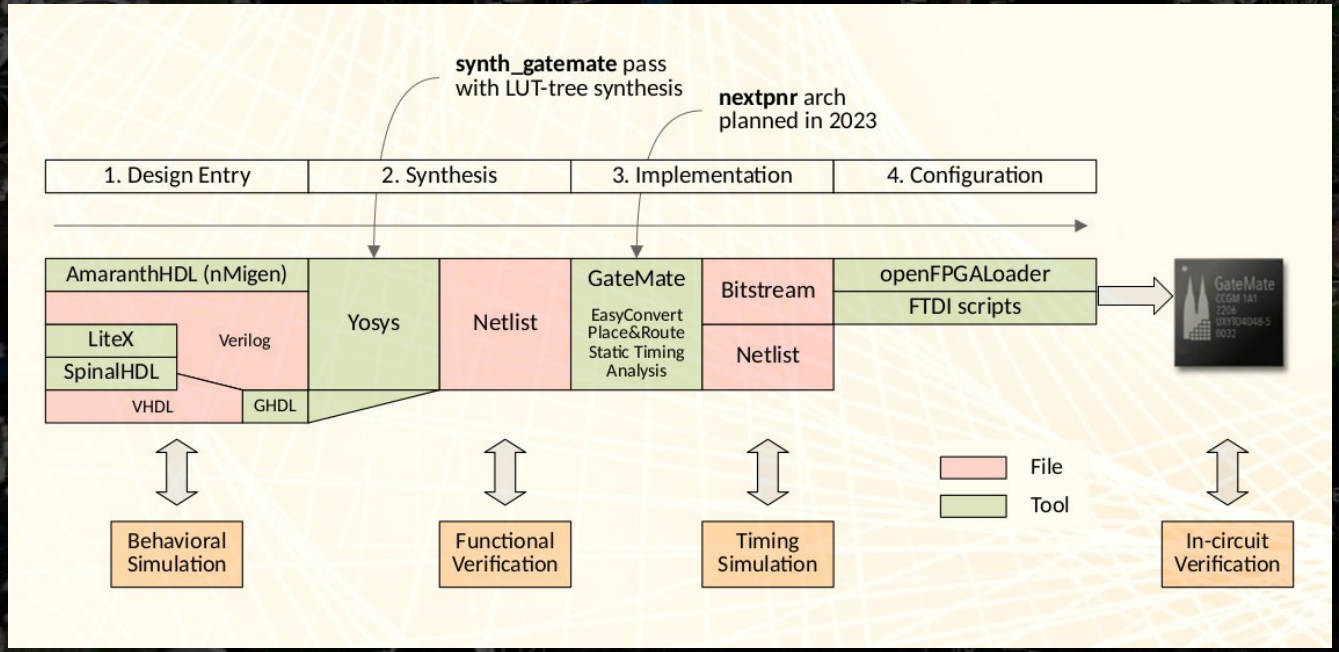
Open Software | **Open Hardware** | Open Standards | Open Data

The Linux Foundation provides a neutral, trusted home for developers to collaborate on open hardware projects. See all open hardware projects.

RISC-V · CHIPS ALLIANCE · CLUSTERDUCK PROTOCOL · pixhawk · OpenPOWER · OPEN 19

New mid range FPGA?

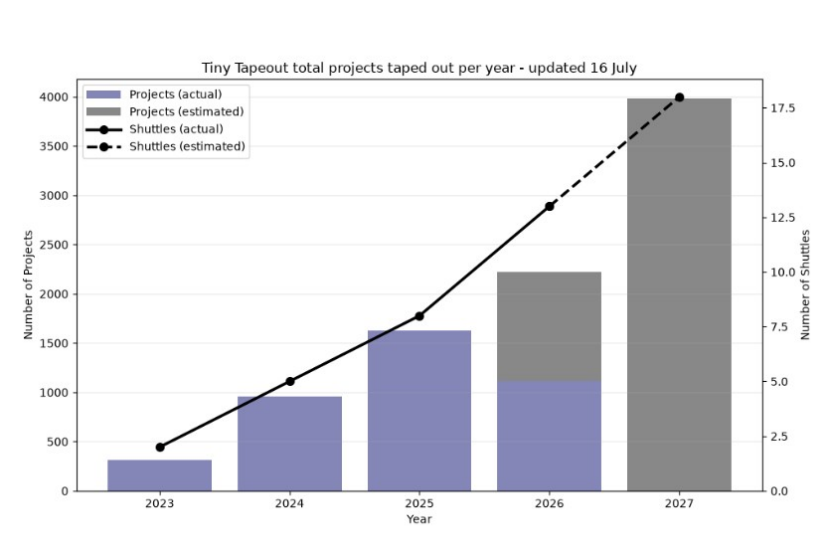
Cologne Chip

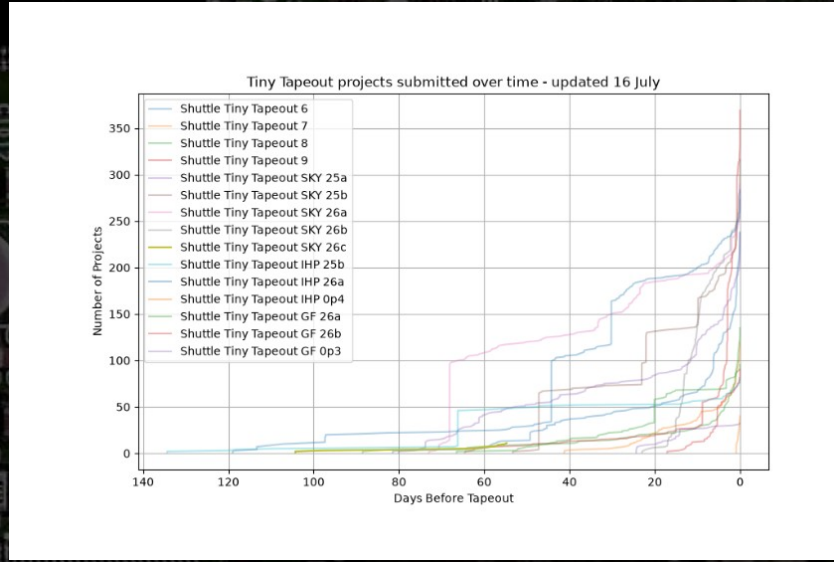


Intro to Tiny Tapeout

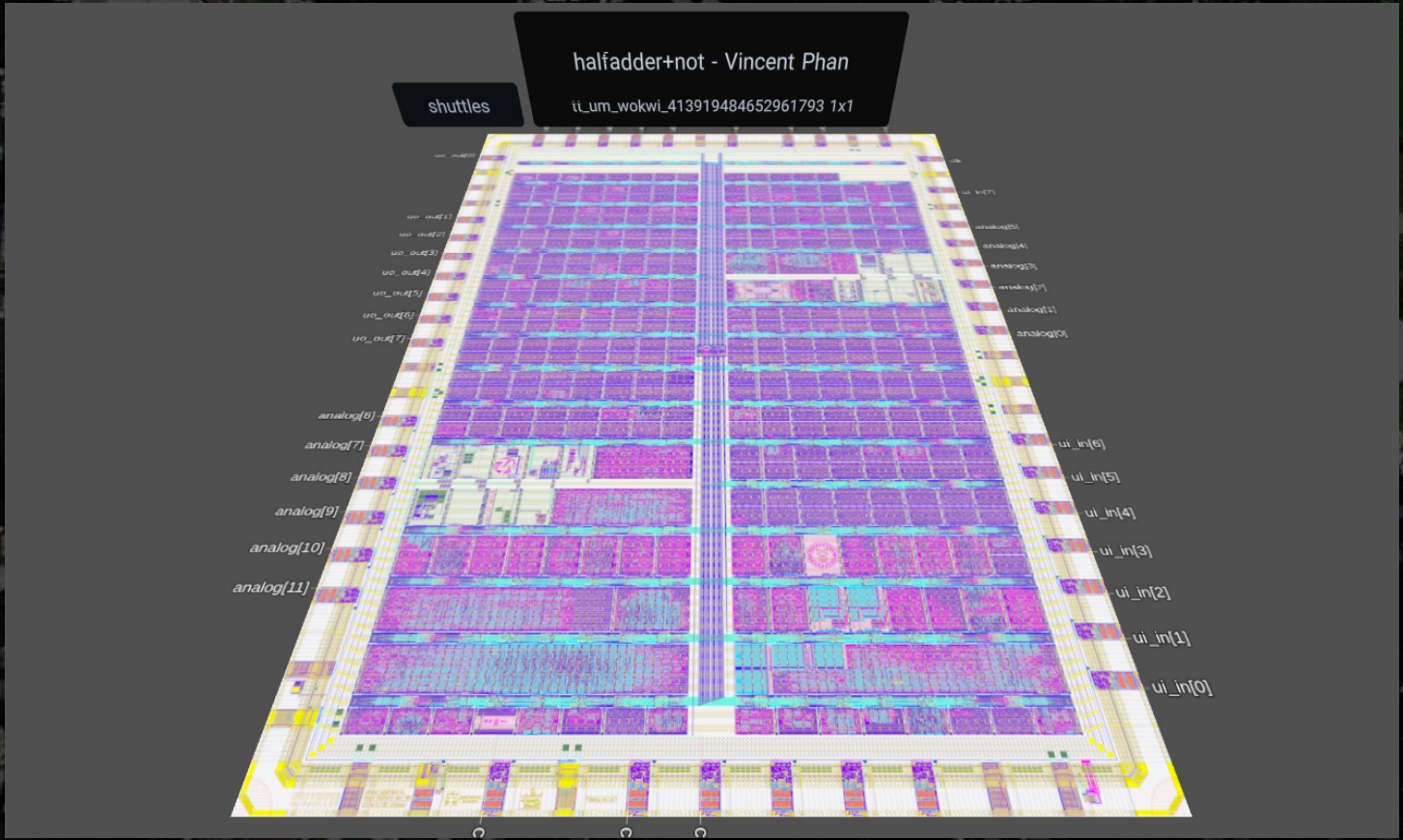


Tiny Tapeout plan 2026-27

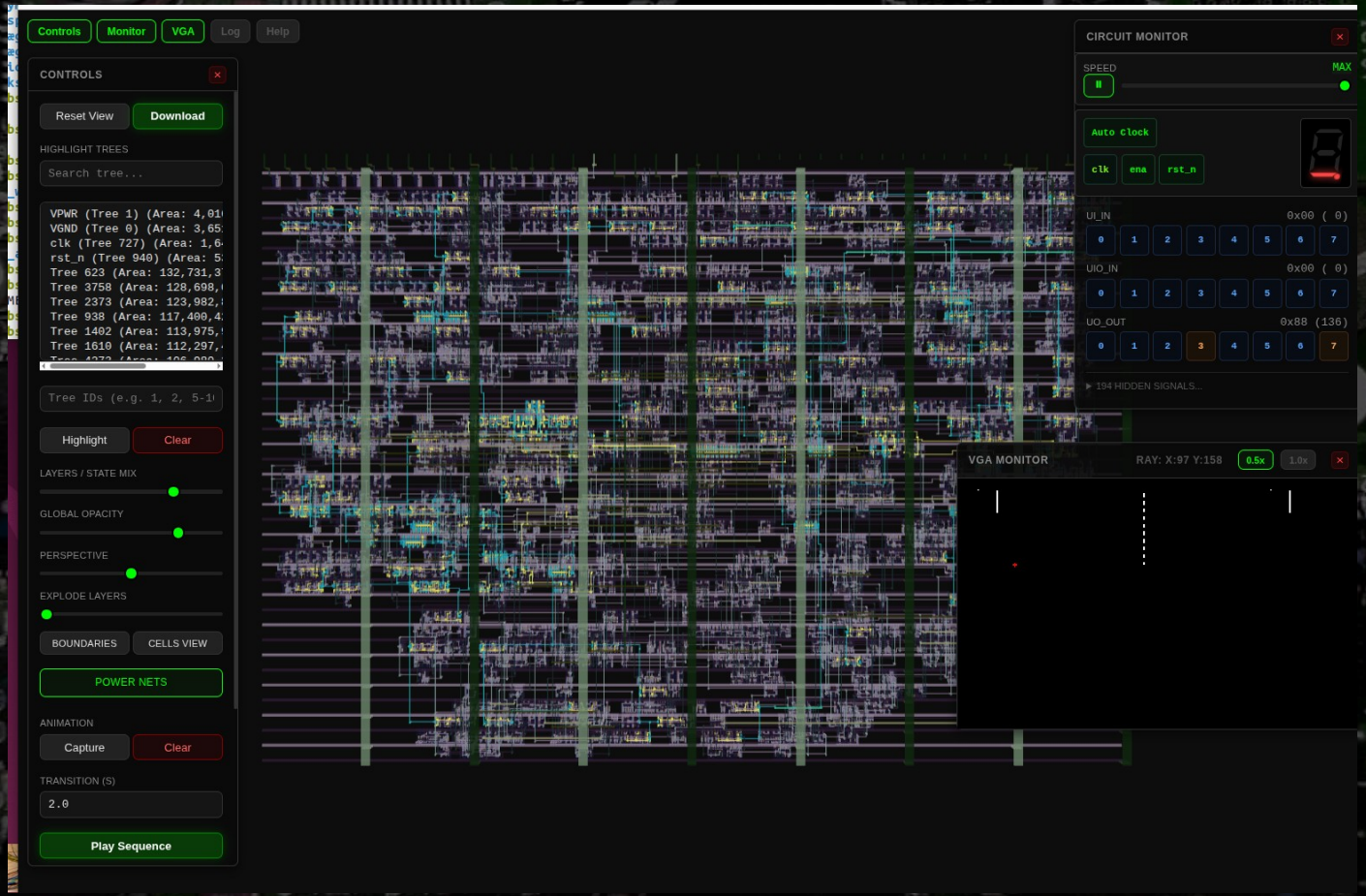




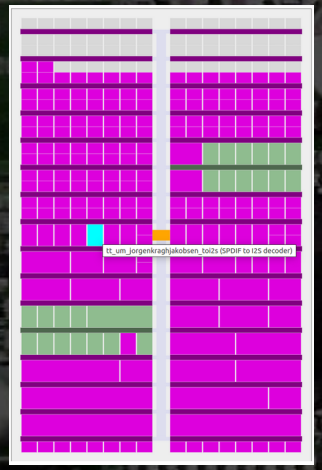
View all (16) TT chips in VR



New tools like TT explorer



Some year ago ...



Same Workshop

Sweatshops and a linked group

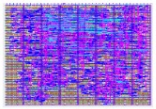
3 designs was tapeout on TT06

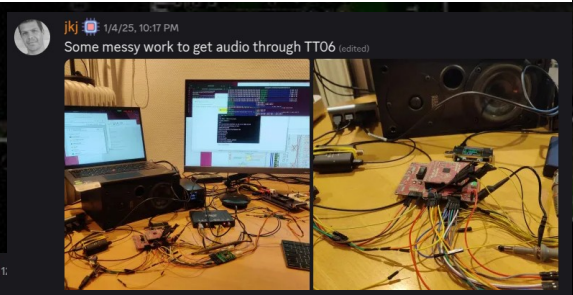
December 2024 Bring Up Party

Audio demo, 4x4 mult., pong game and giveaways

168 : LED PWM controller

- Author: Mikkel Holm Olsen
- Description: Exponential LED PWM controller
- GitHub repository
- Open in 3D viewer





TT06 demos

https://tinytapeout.com/runs/tt06/ To see list of all designs

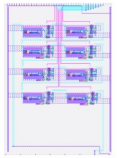
https://commander.tinytapeout.com To control the demoboard

8 : Chisel Pong

- Author: Tjark Petersen
- Description: A basic Pong game using VGA implemented in Chisel.
- GitHub repository
- Open in 3D viewer
- Clock: 50000000 Hz

518 : Integrated Distorion Pedal

- Author: Nanik Adnani
- Description: A simple distortion pedal circuit - taped out! (hopefully)
- GitHub repository
- Open in 3D viewer
- Clock: 0 Hz
- Feedback: 🟡 1

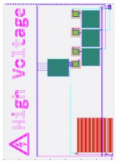


167 : *NOT WORKING* HP 5082-7500 Decoder

- Author: Per Jensen
- Description: Trying to recreate the decoding logic in the HP 5082-7500-display. At this moment project is not finished.
- GitHub repository
- Open in 3D viewer
- View in Wokwi
- Clock: 0 Hz

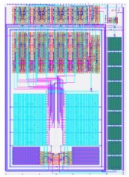
269 : Dickson Charge Pump

- Author: Uri Shaked
- Description: Pumps the input voltage up to ~5.4V
- GitHub repository
- Open in 3D viewer
- Clock: 0 Hz
- Feedback: ✅ 2



231 : TT06 8-bit SAR ADC

- Author: Carsten Wulff
- Description: 8-bit Successive Approximation Register ADC
- GitHub repository
- Open in 3D viewer
- Clock: 4000000 Hz
- Feedback: ✅ 2



Lets try some designs

4x4 signed unsigned multiplier

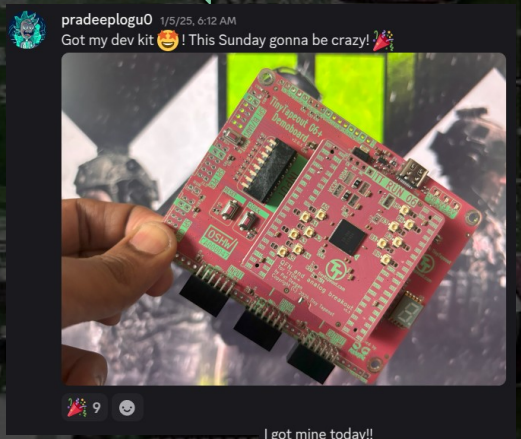
Simon says

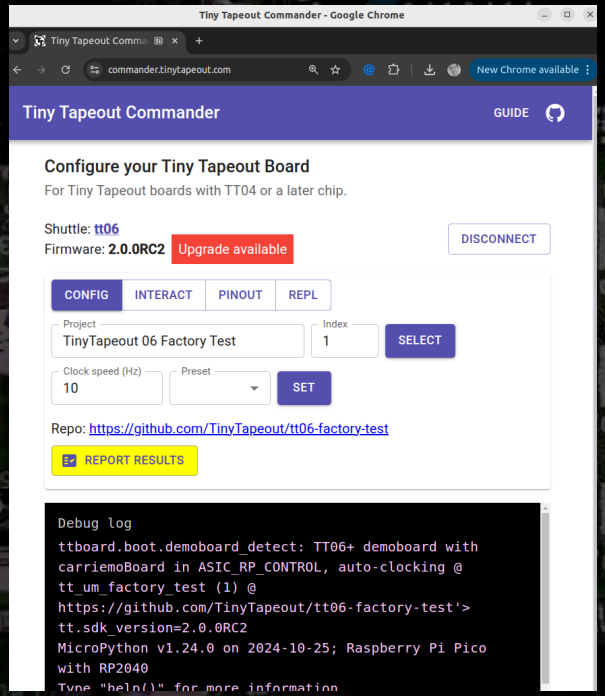
Boot linux

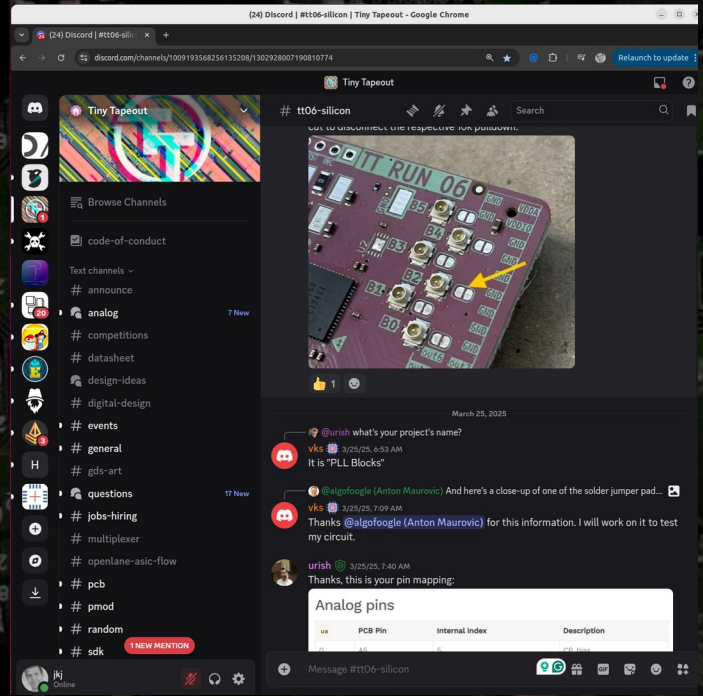
TT06 demo

https://tinytapeout.com/runs/tt06/ To see list of all designs

https://commander.tinytapeout.com To control the demoboard







TT06 demo

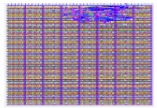
https://tinytapeout.com/runs/tt06/ To see list of all designs

https://commander.tinytapeout.com To control the demoboard

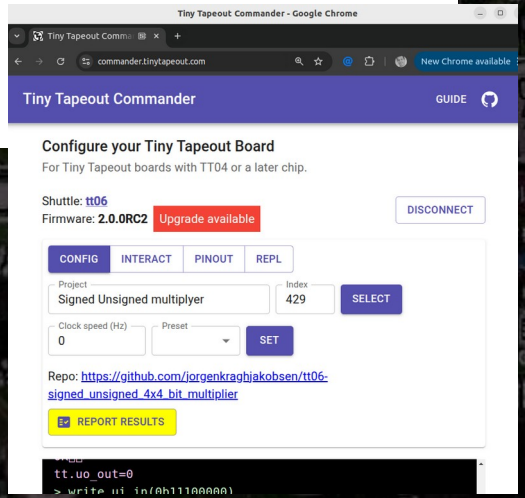
https://tinytapeout.com/runs/tt06/tt_um_signed_unsigned_4x4_bit_multiplier

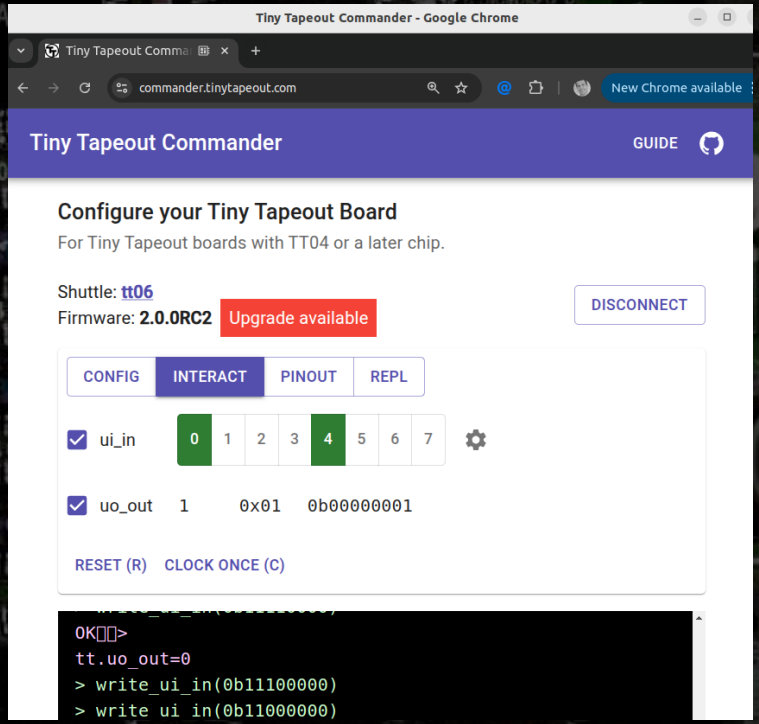
429 : Signed Unsigned multiplyer

- Author: Ole Henrik Moller
- Description: Do a 4x4 multiplication
- GitHub repository
- Open in 3D viewer
- Clock: 0 Hz
- Feedback: ✅ 1



How it works





SCAN ME

TT06 demo

https://tinytapeout.com/runs/tt06/ To see list of all designs

https://commander.tinytapeout.com To control the demoboard

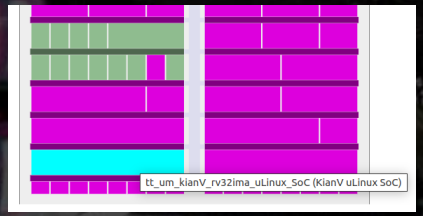
https://www.tinytapeout.com/runs/tt06/tt_um_kianV_rv32im

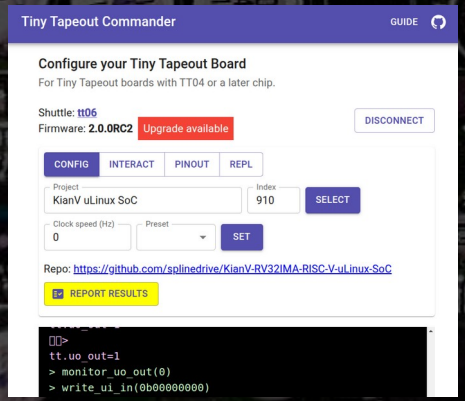
https://tinytapeou

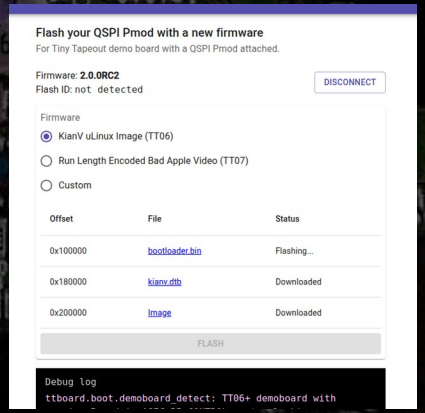
tinytapeout-flasher

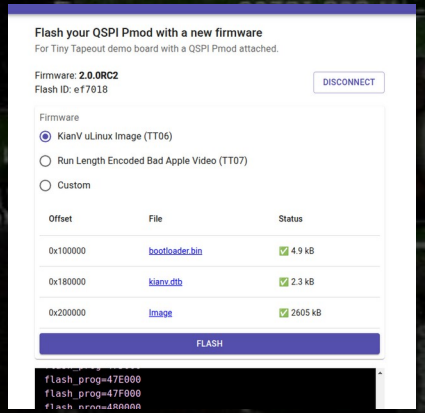


Back to commander, enable tty, reset !

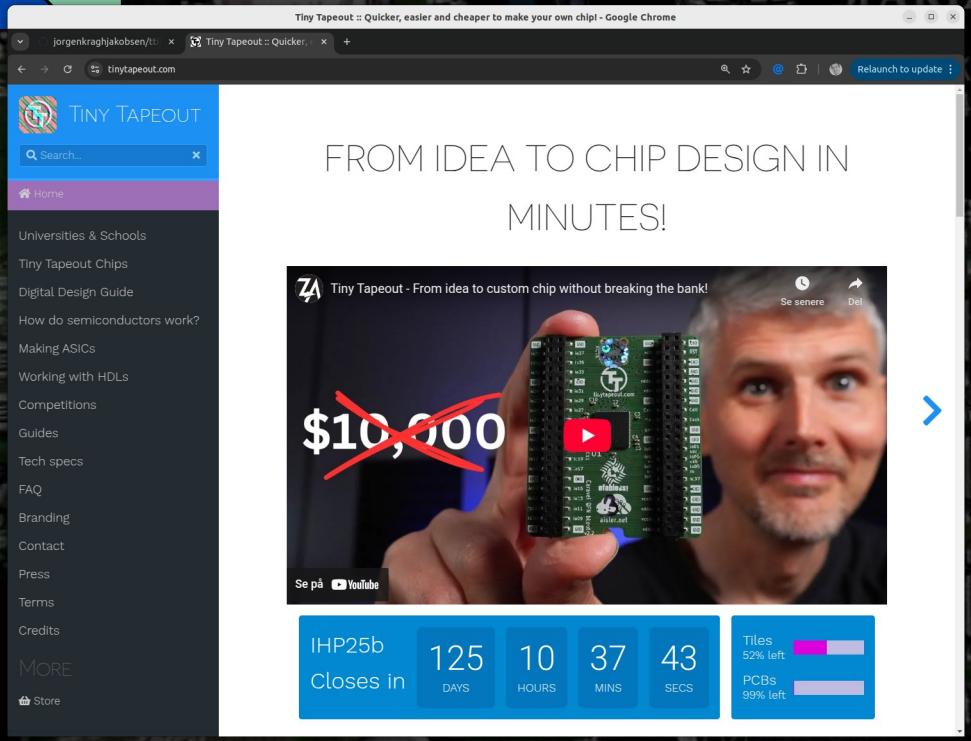


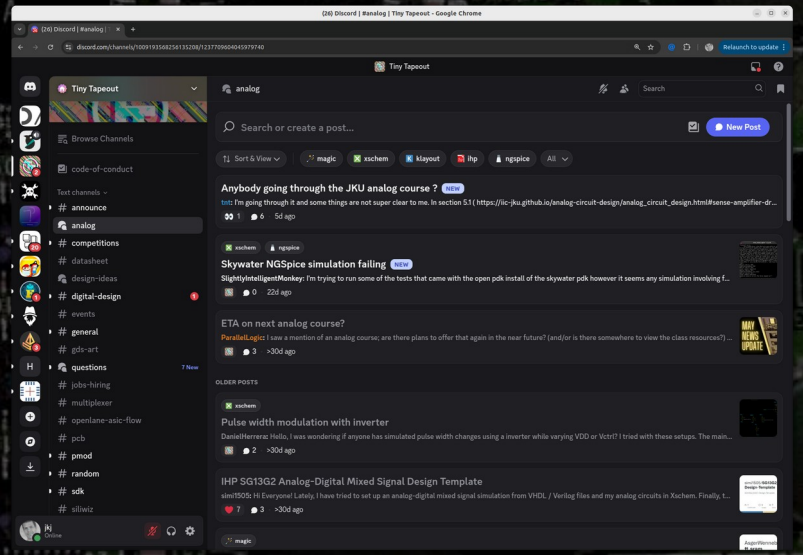






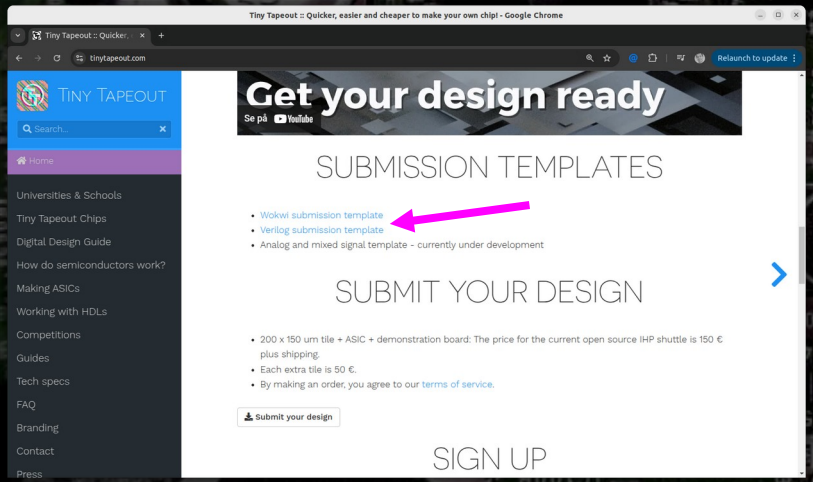
Tiny Tapeout 101

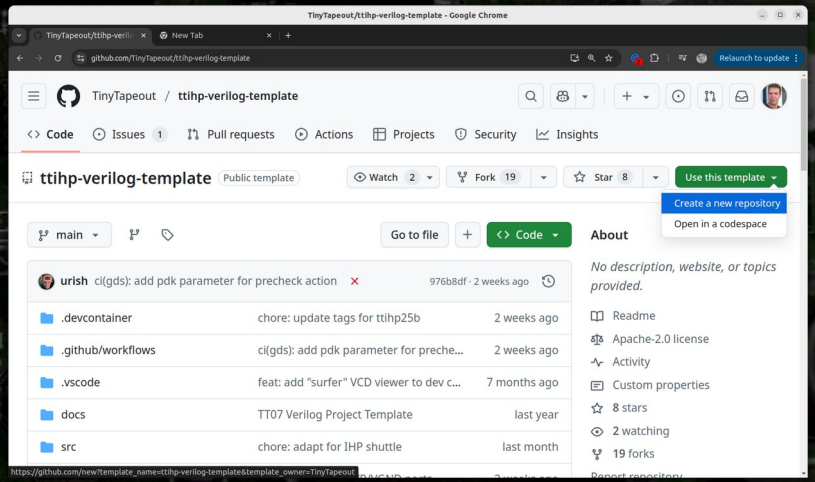




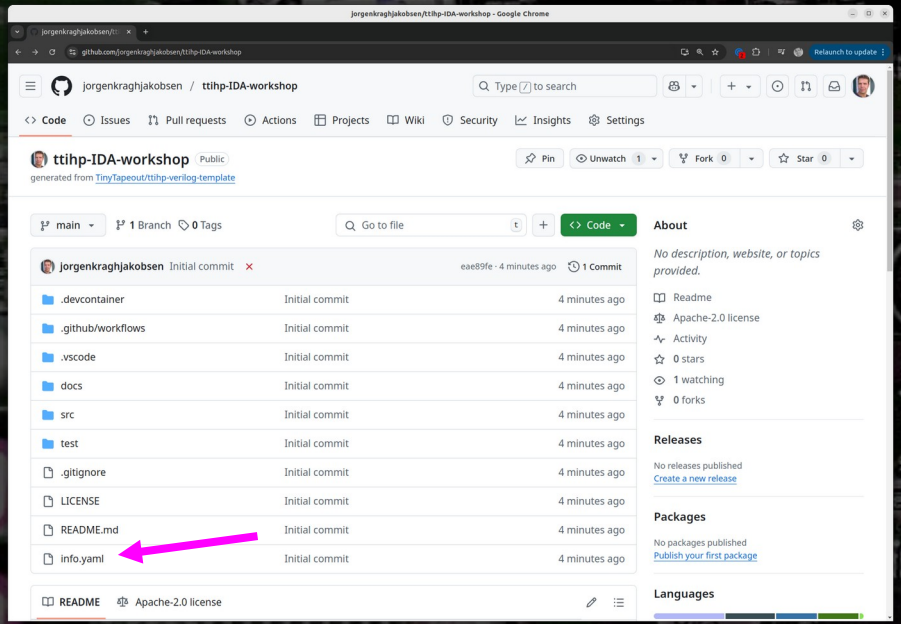
Tiny Tapeout 101

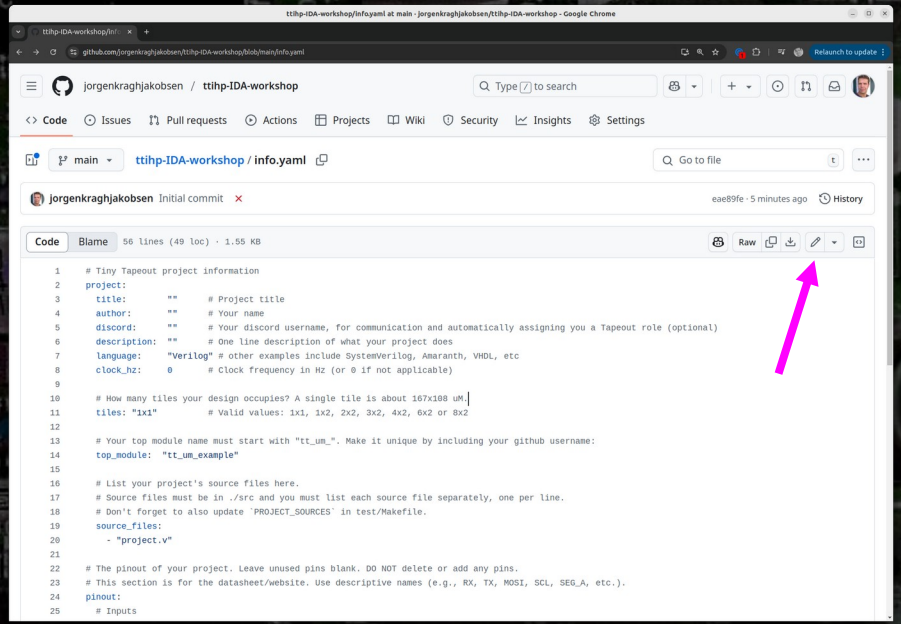
1. Use this template -> Create a new repo





Tiny Tapeout 101
2.a Edit info.yaml with your project details





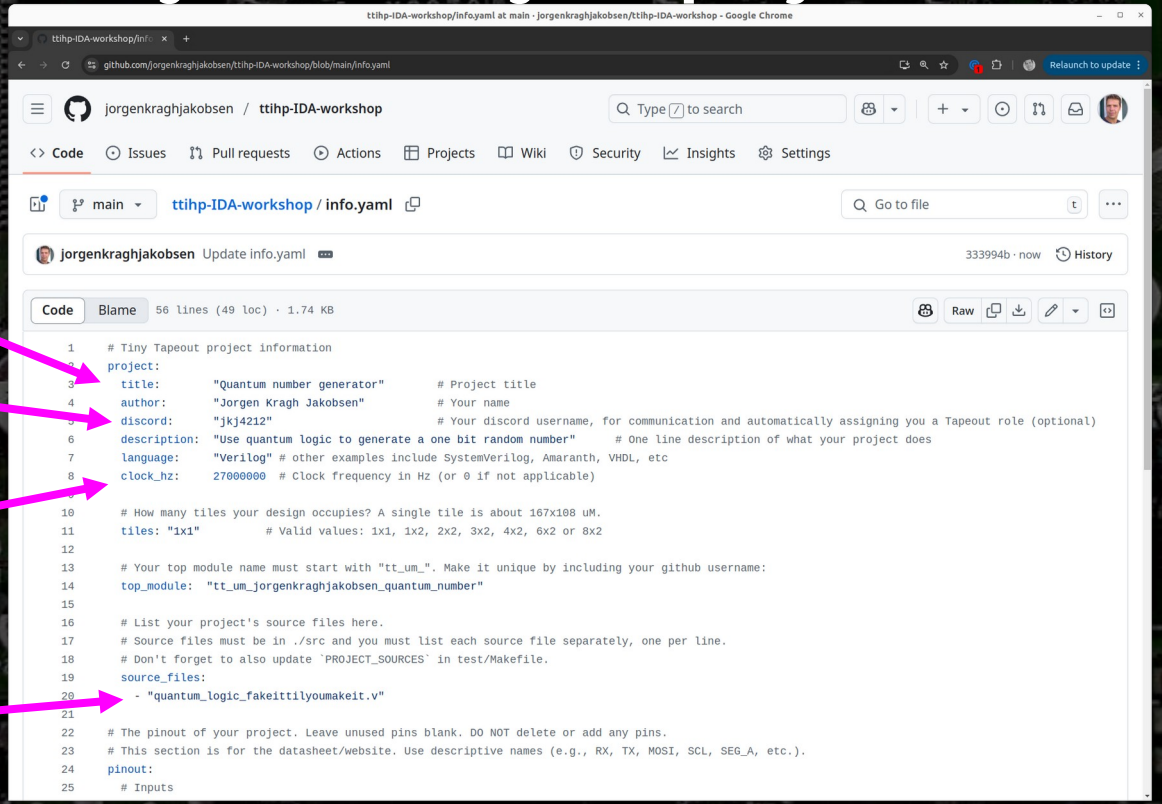
Tiny Tapeout 101
2.b Edit info.yaml with your project details

Title + Name:

Discord:
Automation
Project validation

Clock frequency:
Auto setup for demo
board when selected

verilog source:

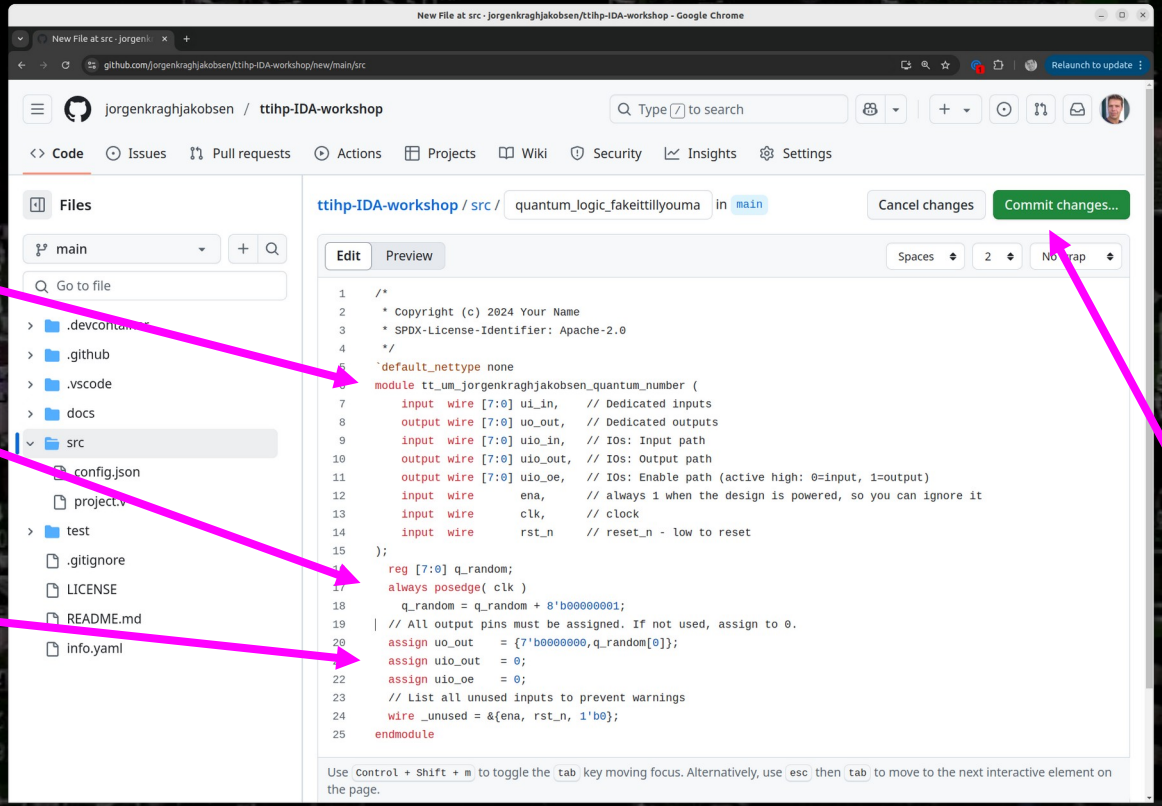


Tiny Tapeout 101
3. Write some Verilog code

Module to be placed at higher level:

Core quantum random logic:

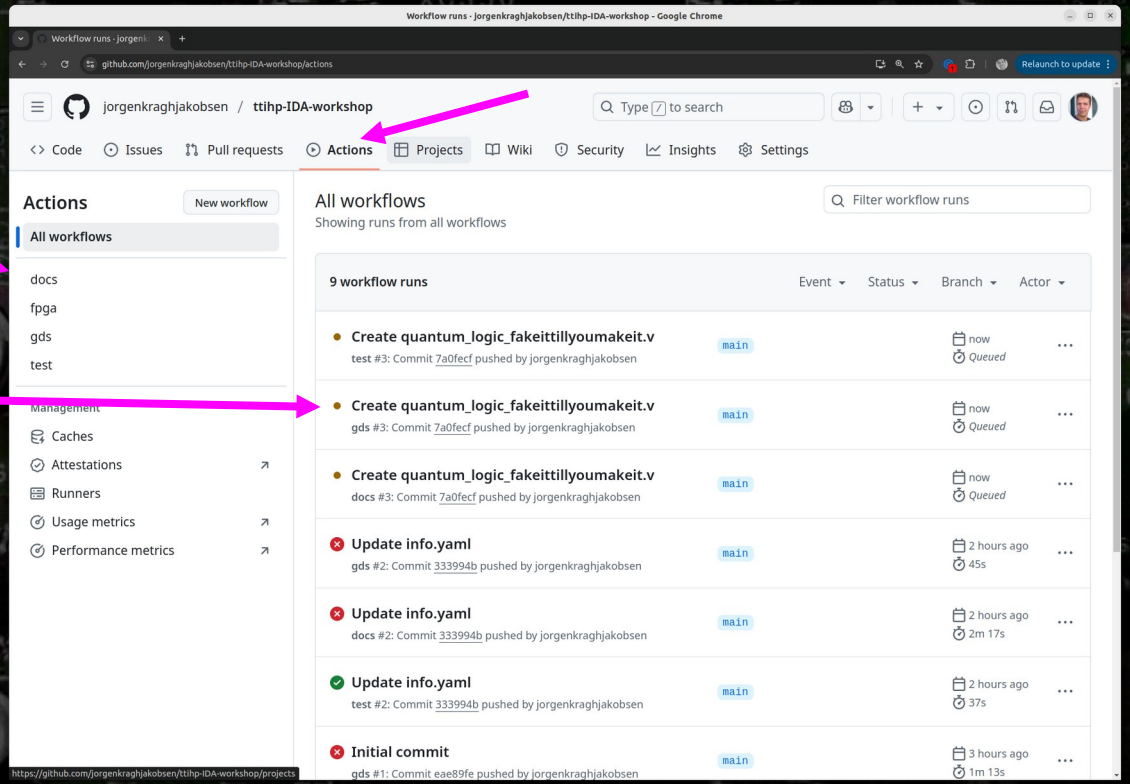
Assign internal signals to general module interface:



Tiny Tapeout 101
4. Commit to start github actions

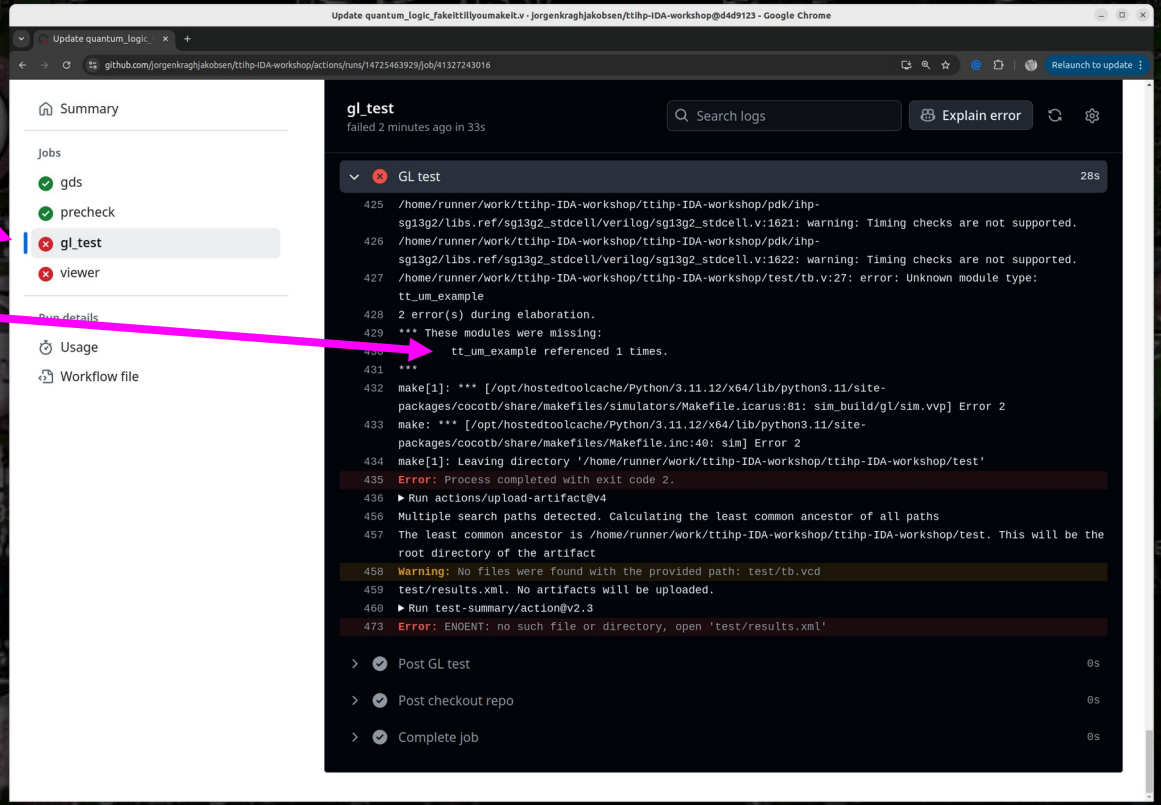
Github actions running:

Look at each action: procedure, progress, log

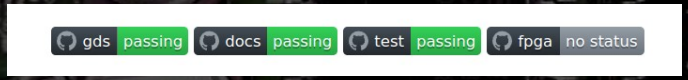


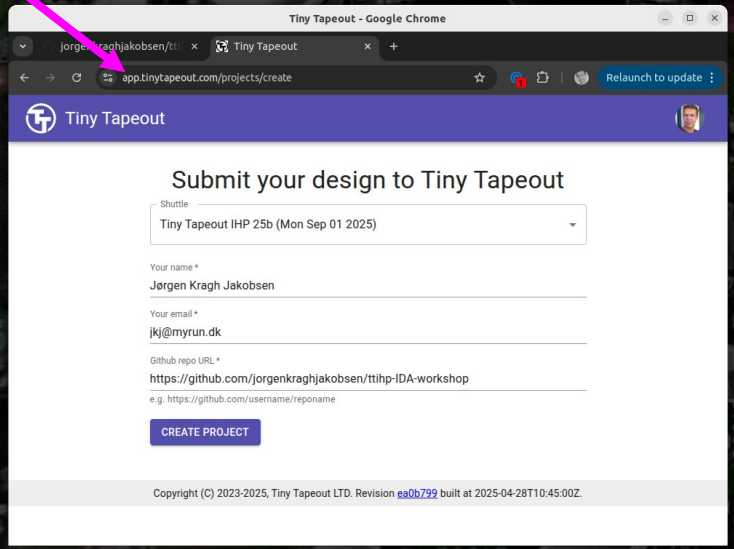
Tiny Tapeout 101
5. Fix errors flagged in actions logs

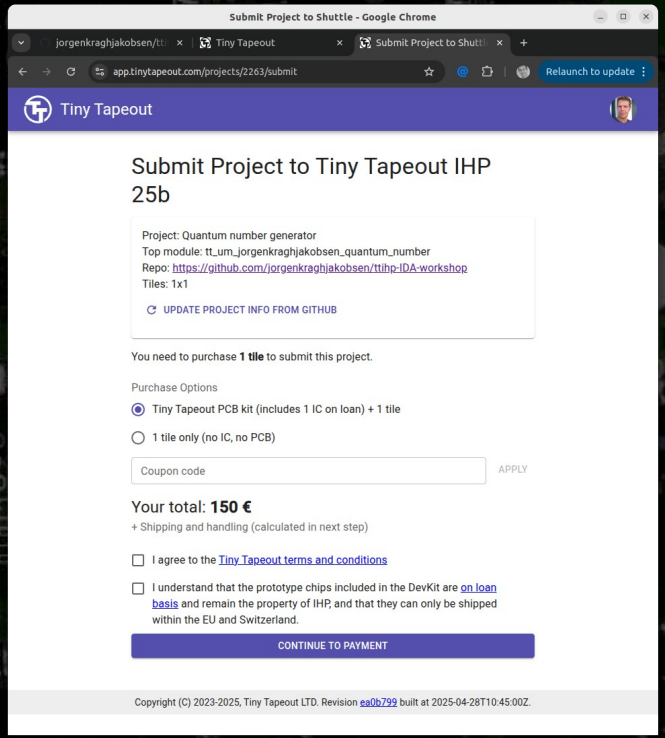
gl_test:
Gatelevel test fails
tt_um_example not updated to new module name



Tiny Tapeout 101
6. All green labels - your are done - go submit

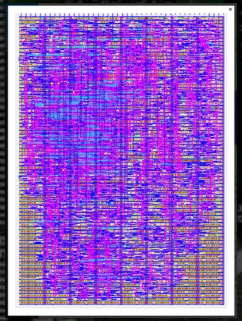


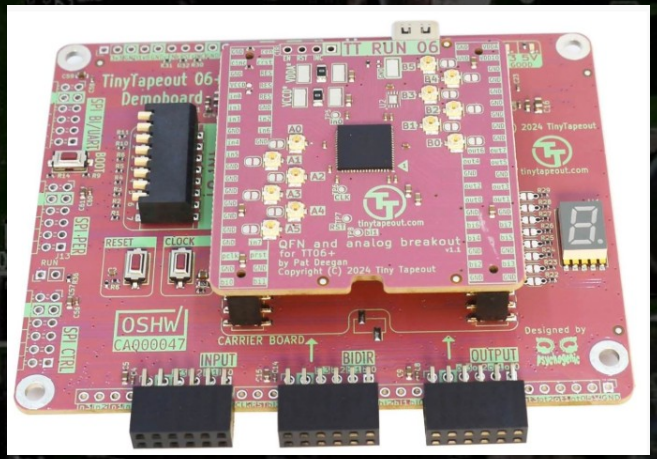




Chip map


tt_um_jorgenkraghjakobsen_toi2s (SPDIF to I2S decoder)

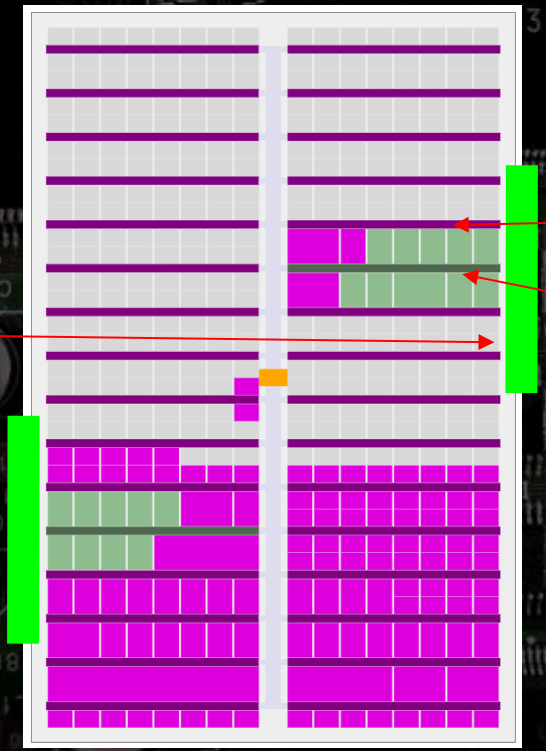



TT RUN 06
TinyTapeout 06
Demoboard
QFN and analog breakout
for TT06+
by Pat Deegan
Copyright (C) 2024 Tiny Tapeout
OSHW
CA000047
CARRIER BOARD
INPUT
BIDIR
OUTPUT
Designed by

Full custom (Analog) on a Tiny Tapeout

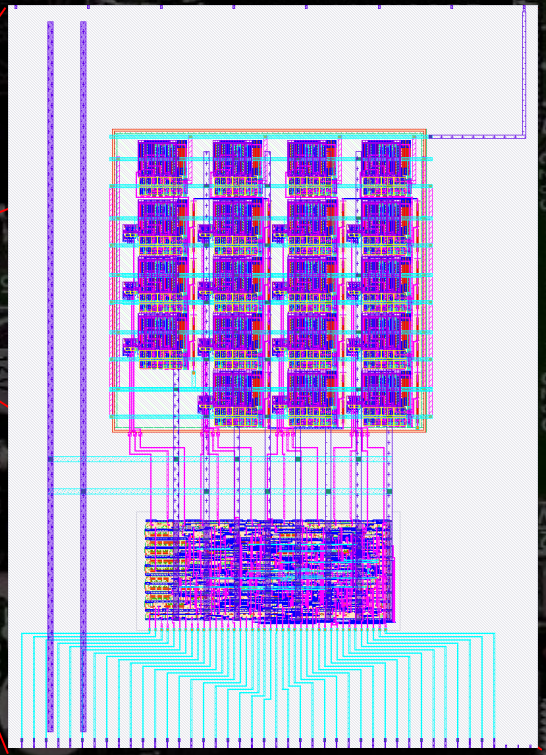
Tiles: “1x2” or “2x2”

set in info.yaml



Full custom on a Tiny Tapeout



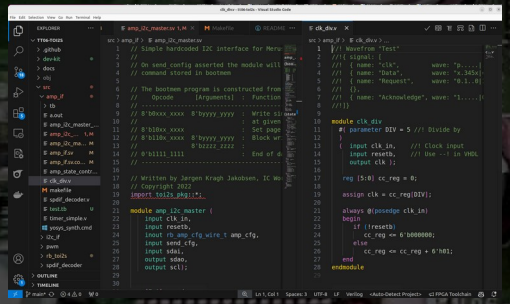


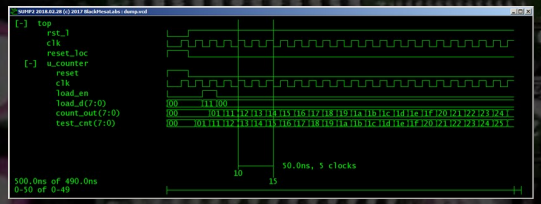
Analog bus

Digital bus

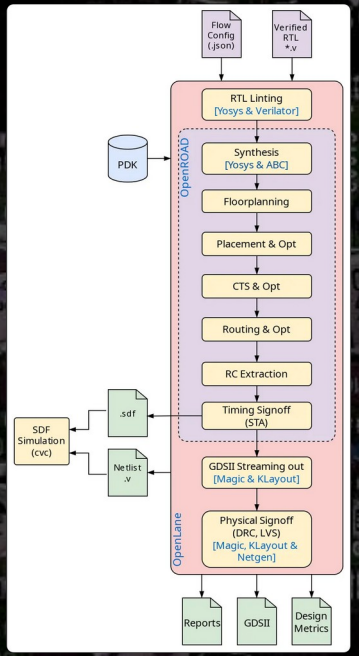
Digital Tiny Tapeout

RTL





TT FLOW

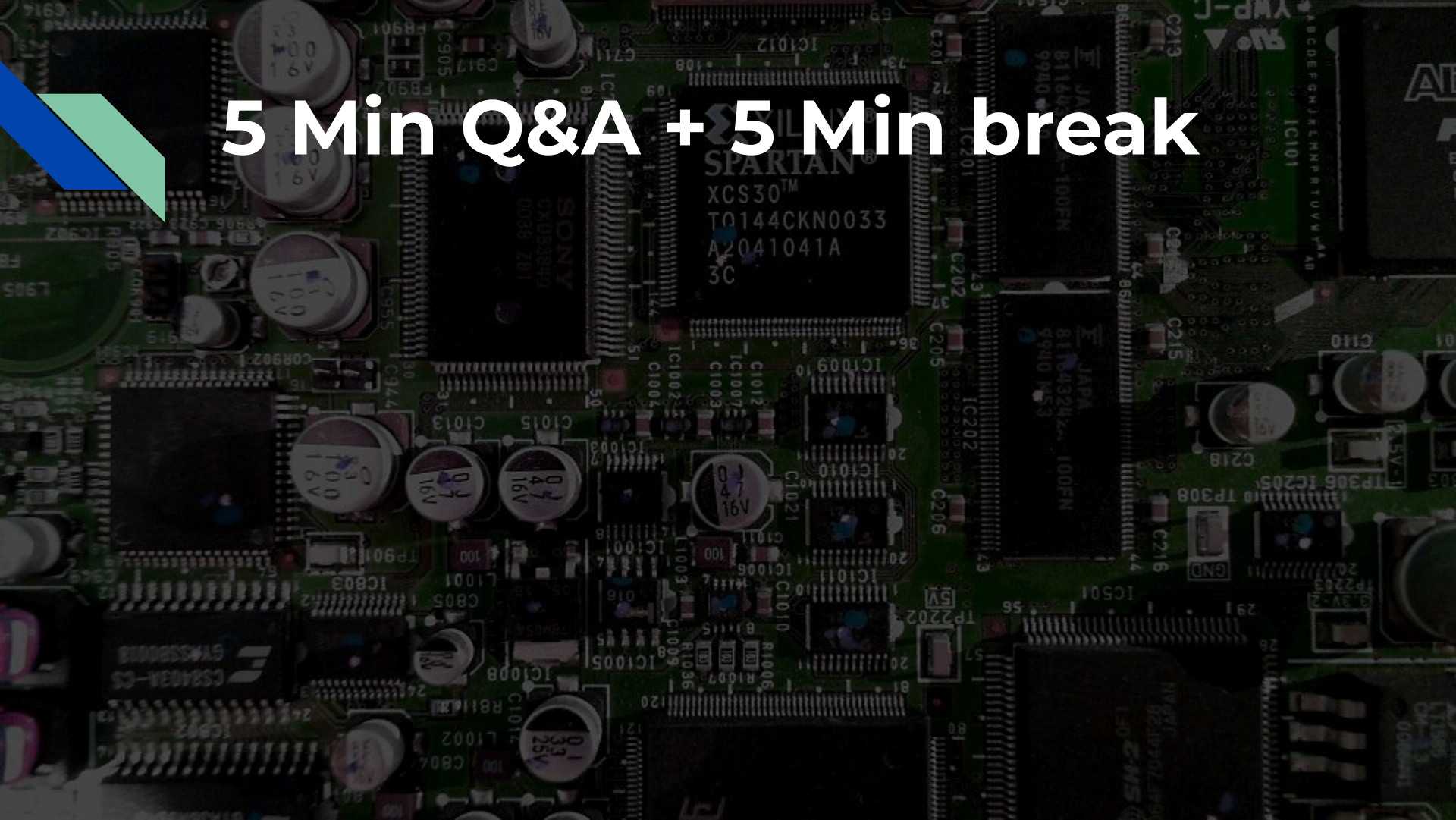


fixed
Floorplan
CTS
Buffers
Antennas
errors

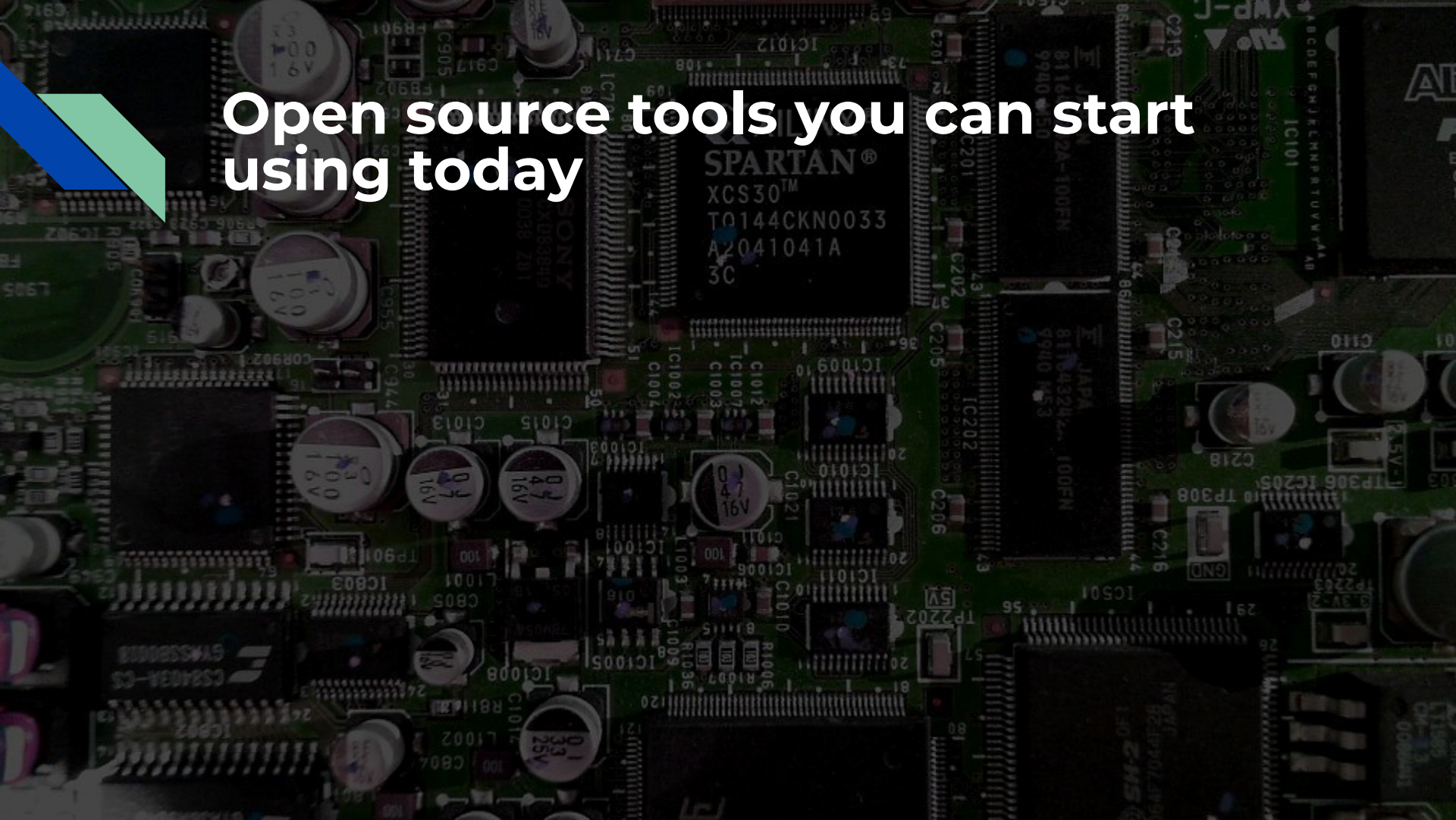
GDS



LVS + DRC
by design


5 Min Q&A + 5 Min break

Open source tools you can start using today



Open source tools you can start with

Digital frontend:

- yosys
- iverilog
- verilator
- gtkwave
- cocotb

Digital backend:

- OpenROAD-flow-script - will pull OpenROAD
- klayout
- magic

Analog tools:

- Use this guide https://github.com/bluecmd/learn-sky130
- Xschem,
- ngspice
- gaw or beSpice wave from Analog Flavor https://www.analogflavor.com/en/bespice/software-downloads/

Install PDKs

Install the volare from efabless

https://github.com/efabless/volare

Follow install procedure procedure

and install sky130 lastest

Digital design frontend

RTL design in text/code editor

Verilog, SystemVerilog, VHDL, XLS,

Chisel, Amaranth HDL, TL-Verilog

Functional verification using digital simulator

Verilator, Icarus Verilog and GHDL

Validation tools

Formal, Cocotb and Gtkwave

Digital backend

FPGA - Yosys/NextPnR

SpartanX, ICE40, Gowin

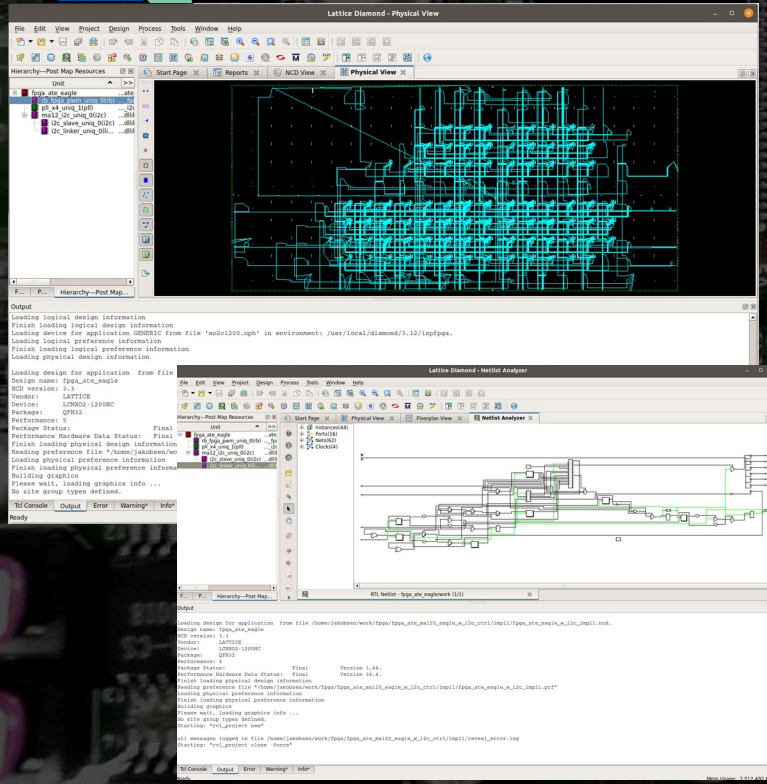
ASIC - Yosys/openRoad/custom

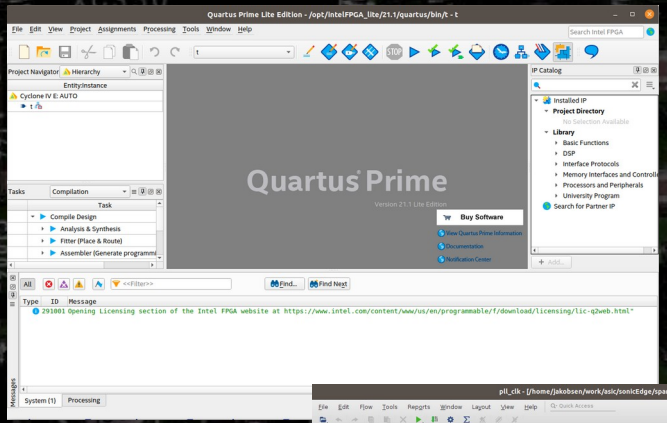
SKY130 / SKY90

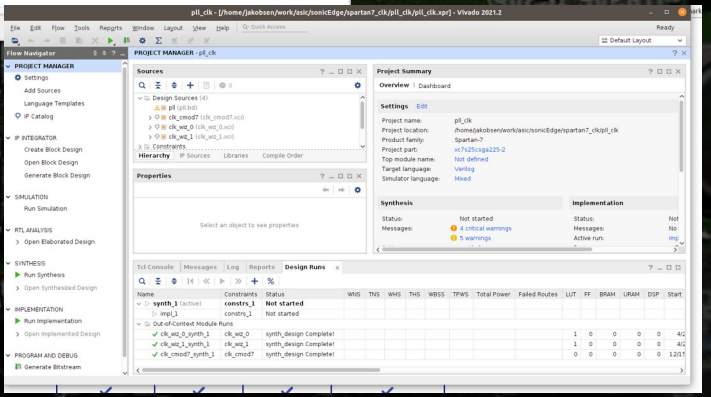
GF180mcu - IHP130

Closed source PDKs

Vendor GUIs


Lattice Diamond - Physical View
Lattice Diamond - Netlist Analyzer


Quartus Prime Lite Edition - /opt/intelFPGA_lite/21.1/quartus/bin/t - t
Quartus Prime


pll_clk - [/home/jakobsen/work/asic/sonicEdge/spartan7_clk/pll_clk/pll_clk.xpr] - Vivado 2021.2

Scripted flows

Automation

Documentation

Custom tools / Flow

Code revision easy to handle

Faster

```
#-----------------------------------------------------------------------
# Synthesis target VIVADO
#-----------------------------------------------------------------------
ifeq ($(SYNTHTOOL),VIVADO)

VIVADO = /opt/Xilinx/Vivado/2021.2/bin/vivado

$(OBJDIR)/%_pins.xdc: $(CURDIR)/%_pins.xdc
	cp -p $< $@

#echo "set_property IS_GLOBAL_INCLUDE 1 [get_files $(filter %.svh,  $(SOURCES_RTL) )]" >> $@


$(OBJDIR)/$(HDL_TOP)_synth.$(SYNTHTOOL).tcl: \
  $(SOURCES_RTL) \
  $(OBJDIR)/$(HDL_TOP)_$(BOARD)_pins.xdc
	echo "set workspace $(WORKSPACE)" > $@
	echo "set objdir $(OBJDIR)" >> $@
	echo "set srcdir $(CURDIR)" >> $@
	echo "set design_name $(HDL_TOP)" >> $@
	echo "set device $(DEVICE)" >> $@
	echo "set_part $(DEVICE)" >> $@
	echo "set pin_map $(PIN_MAP)" >> $@
	echo "set rep_dir ./report" >> $@
	echo "file mkdir ./report" >> $@
	echo "set tmp_dir ./temp" >> $@
	echo "file mkdir ./temp" >> $@
	echo "read_vhdl  -vhdl2008 { $(filter %.vhd , $(SOURCES_RTL)) }" >> $@
	echo "read_verilog -sv { $(filter %.svh %.sv , $(SOURCES_RTL)) }" >> $@
	$(foreach s, $(filter %.v, $(SOURCES_RTL)), echo "read_verilog $(s)" >> $@; )
	echo "read_xdc $(HDL_TOP)_$(BOARD)_pins.xdc" >> $@
	echo "synth_design -top $(HDL_TOP) -part $(DEVICE) -fsm_extraction off" >> $@
	echo "opt_design" >> $@
	echo "power_opt_design -verbose" >> $@
	echo "write_edif -force $(HDL_TOP).edif" >> $@
	echo "place_design -directive Explore" >> $@
	echo "phys_opt_design" >> $@
	echo "route_design -directive Explore" >> $@
	echo "set_property BITSTREAM.CONFIG.USR_ACCESS        0x12345678     [current_design]" >> $@
	echo "set_property CONFIG_VOLTAGE                     3.3            [current_design]" >> $@
	echo "set_property CFGBVS                             VCCO           [current_design]" >> $@
	echo "set_property BITSTREAM.CONFIG.CONFIGRATE        16             [current_design]" >> $@
	echo "set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR    No             [current_design]" >> $@
	echo "set_property SEVERITY {Warning} [get_drc_checks NSTD-1]" >> $@
	echo "write_bitstream -force $(HDL_TOP).bit" >> $@
	echo "write_bitstream -force -bin_file $(HDL_TOP)" >> $@
	echo "write_cfgmem    -force -format MCS -size 8 -loadbit \"up 0x0 $(HDL_TOP).bit\" -interface SPIx1
	echo "exit" >> $@
```

Has anyone tried TerosHDL?

r/FPGA · Posted by u/TheSkyHighPolishGuy Xilinx User 1 year ago

15

Has anyone tried TerosHDL?

I posted recently about my trouble with the Vivado GUI workflow and got tons of advice to switch to a script-driven approach, so I was looking at HDL extensions in the VS Code marketplace to go along with this workflow instead of coding in Vivado. There, I found an extension called TerosHDL that seems quite capable: https://terostechnology.github.io/terosHDLdoc/. There's also a talk from its creators at FOSDEM '21: https://fosdem.org/2021/schedule/event/teroshdl/.

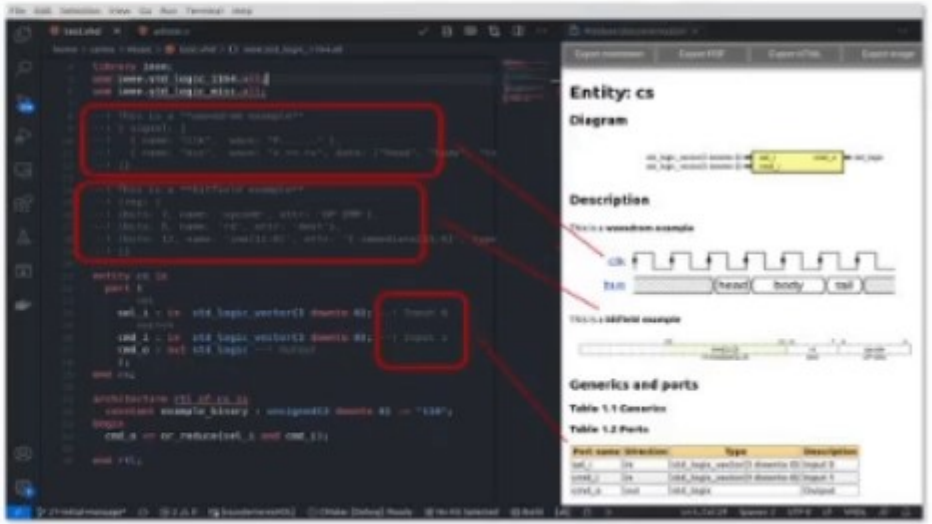
It's rather new, so has anyone tried it?

12 Comments Share Save Hide Report 87% Upvoted

FOSDEM https://fosdem.org/2021/schedule/event/teroshdl/

TerosHDL

- Linter.
- Documentation generator.
- Go to definition.
- Templates.
- Snippets.
- Formatter.
- State machine viewer.
- State machine designer.
- Project manager.
- Dependencies viewer.



TerosHDL

Short demo

my code in work/asic/integrated_speaker

Formater

Documenter - wavedrom

Schematics

State machine

Templets - testbenchs

https://terostechnology.github.io/terosHDLdoc/

TOOLS for Open source FPGA flows

Yosys : https://github.com/YosysHQ/yosys

NextPNR : https://github.com/YosysHQ/nextpnr

OpenFPGAloader : https://github.com/trabucayre/openFPGALoader

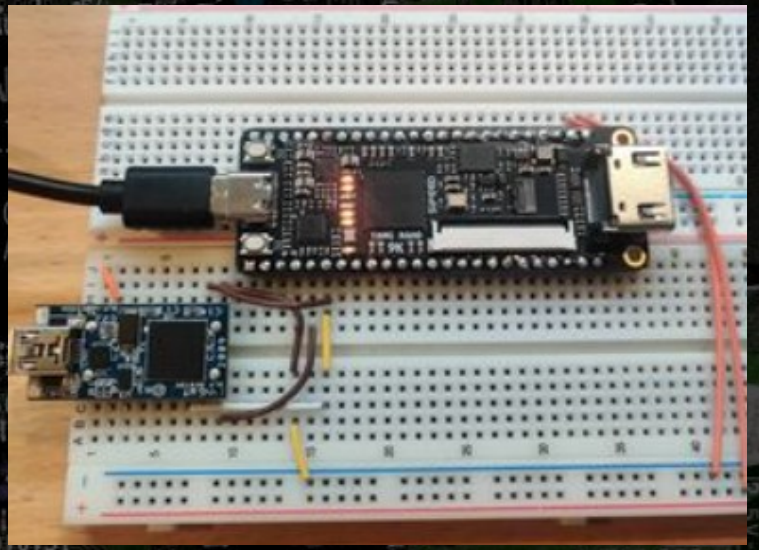
install - from package manager or compile from source

https://github.com/YosysHQ/yosys#getting-started

https://www.mehmetburakaykenar.com/synthesis-n-bit-counter-with-open-source-yosys-synthesizer/294/

Work with FPGA

```
#-----------------------------------------------------------------------
# FPGA Target
#-----------------------------------------------------------------------

all_fpga: synth place bit load

# Synthesis
$(PRO).json: $(PRO).sv
    yosys -p " \
    read_verilog ../amp_i2c_master/clk_div.v ; \
    read_verilog ../amp_i2c_master/amp_i2c_master.v ; \
    read_verilog ../amp_state_control/timer_simple.v ; \
    read_verilog ../amp_state_control/amp_state_control.v ; \
    read_verilog -sv ../spdif_decoder/spdif_decoder.sv ; \
    read_verilog -sv $(PRO).sv ; \
    synth_gowin -top $(PRO) -json $(PRO).json"

# Place and Route
$(PRO)_pnr.json: $(PRO).json
    nextpnr-gowin --json $(PRO).json --freq 27 --write $(PRO)_pnr.json \
    --device ${DEVICE} --family ${FAMILY} --cst ${BOARD}.cst

# Generate Bitstream
$(PRO).fs: $(PRO)_pnr.json
    gowin_pack -d ${FAMILY} -o $(PRO).fs $(PRO)_pnr.json

# Program Board flash or RAM
flash: $(PRO).fs
    $(OFL) -b ${BOARD} $(PRO).fs -f

load: $(PRO).fs
    ${OFL} -b ${BOARD} $(PRO).fs
```



Tangnano 9k and 20k from Sipeed

Digital Chip design

Design ideas
New - Faster
Cheaper

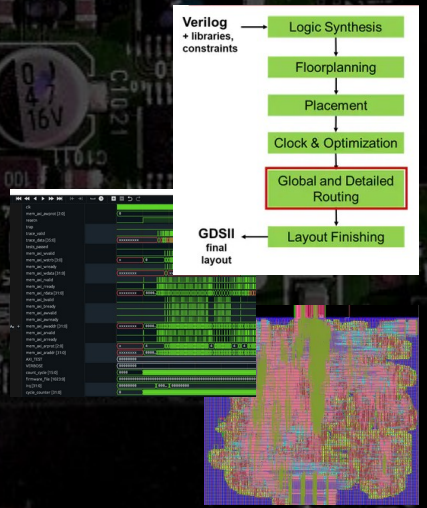
Architecture
Concept
Model/Design

Implementation
PDK
Simulation

Prototype
MPW
Tinytapeout

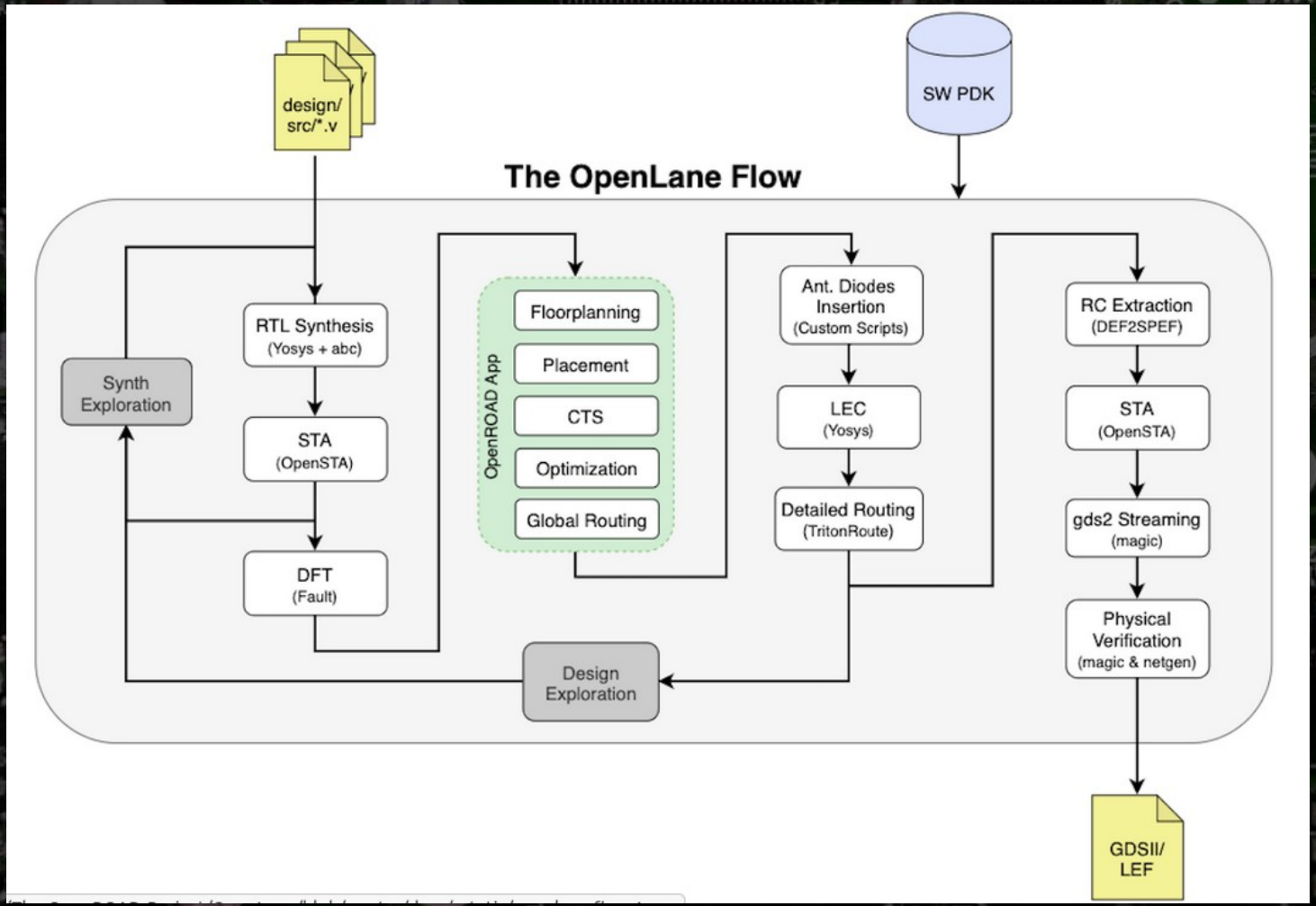
Domain knowledge
Size, cost
performance

Model Octave
Python
VHDL/Verilog/SV

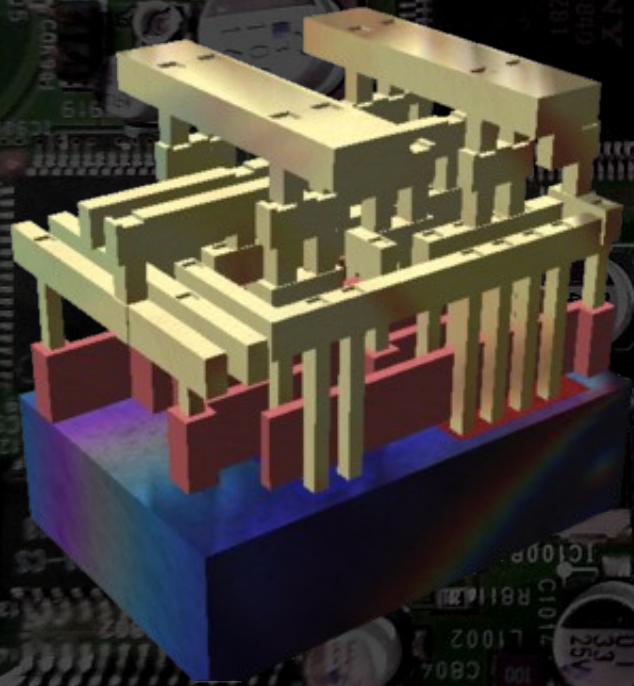


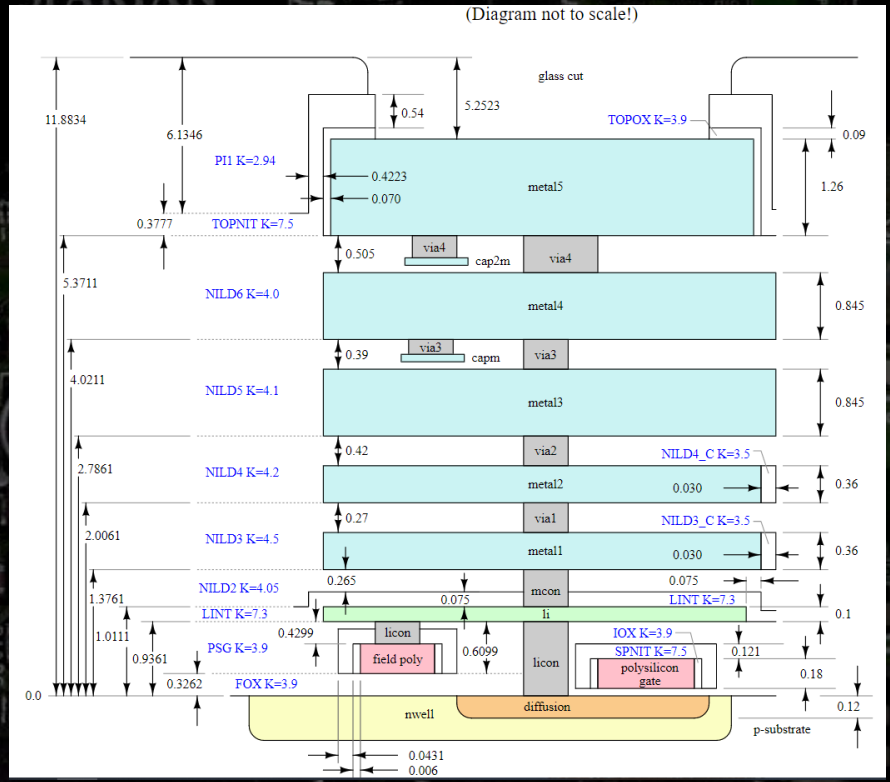
Design submission
Metal fill
Signoff check
DRC waiver

integration
A + B + C
in single chip

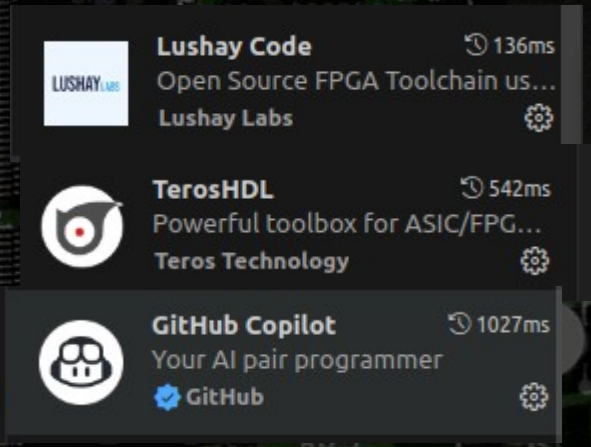

design/
src/*.v
SW PDK
The OpenLane Flow
RTL Synthesis
(Yosys + abc)
Synth
Exploration
STA
(OpenSTA)
DFT
(Fault)
OpenROAD App
Floorplanning
Placement
CTS
Optimization
Global Routing
Ant. Diodes
Insertion
(Custom Scripts)
LEC
(Yosys)
Detailed Routing
(TritonRoute)
RC Extraction
(DEF2SPEF)
STA
(OpenSTA)
gds2 Streaming
(magic)
Physical
Verification
(magic & netgen)
Design
Exploration
GDSII/
LEF

Standard cells and Process layers sky130



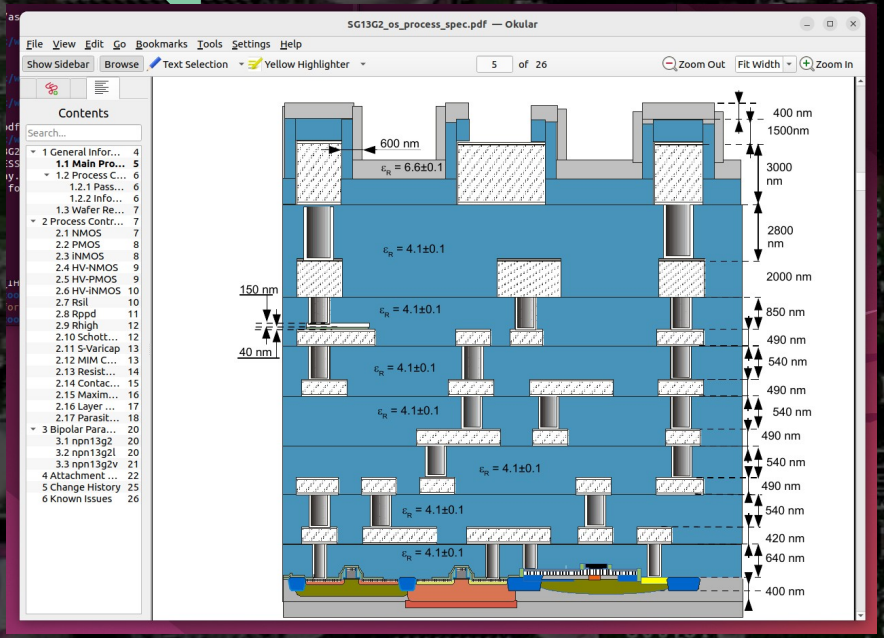


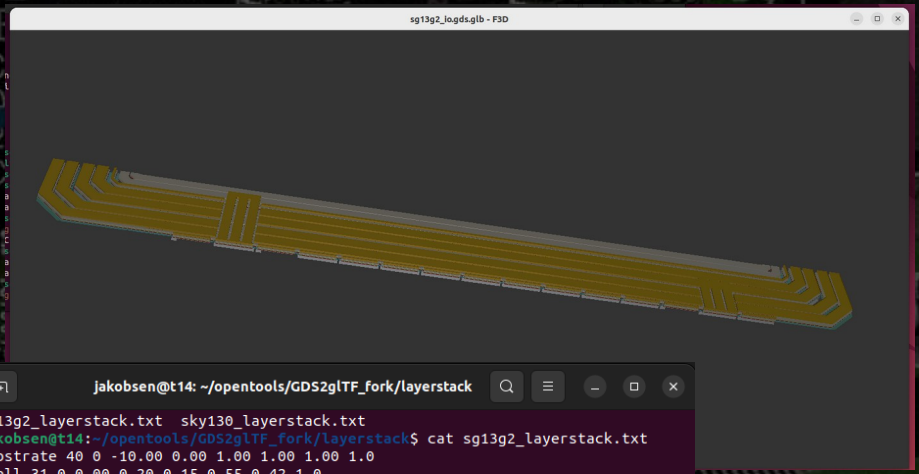
Verilog development with VS code



- Install VScode
- Copilot - LLM to help
- Install extensions: Lushay Code, TerosHDL
- TerosHDL
  - Linting, syntax highlight, schematic/state machine viewer
    - Custom setup for supported tools
- Lushay Code
  - GOWIN FPGA helpers - config files gui

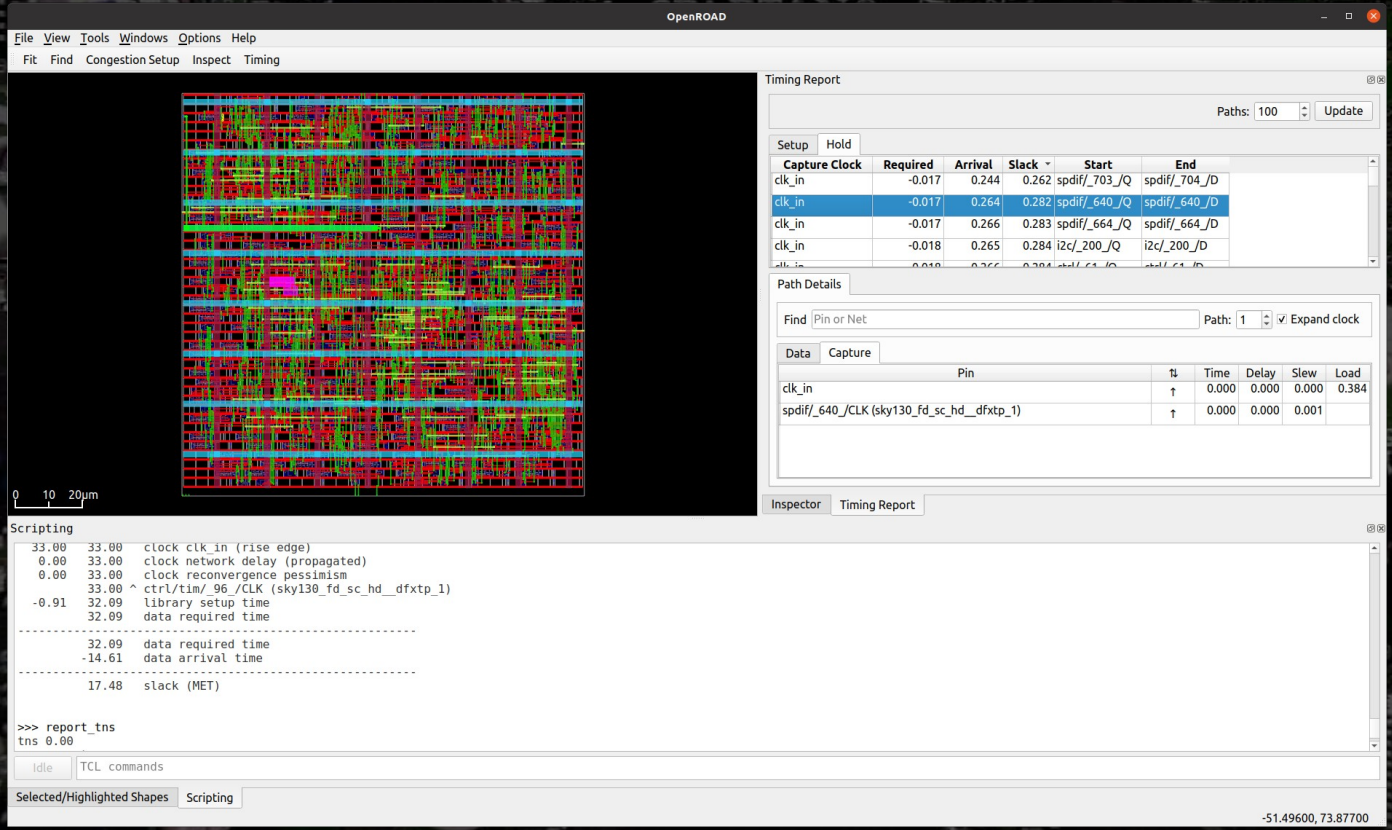
Layer stack and 3D images of layout






```
jakobsen@t14: ~/opentools/GDS2glTF_fork/layerstack
sg13g2_layerstack.txt  sky130_layerstack.txt
jakobsen@t14:~/opentools/GDS2glTF_fork/layerstack$ cat sg13g2_layerstack.txt
Substrate 40 0 -10.00 0.00 1.00 1.00 1.00 1.0
NWell 31 0 0.00 0.20 0.15 0.55 0.42 1.0
PWell 46 0 0.00 0.20 1.00 1.00 0.00 1.0
Active 0 0 0.20 0.32 0.00 0.00 0.00 1.0
ResPoly 0 0 0.32 0.42 0.00 0.00 0.00 1.0
GatPoly 5 0 0.32 0.42 0.75 0.25 0.15 1.0
Cont 6 0 0.32 0.96 0.00 1.00 1.00 1.0
Metal1 8 0 0.93 1.33 0.22 0.75 1.00 1.0
Via1 19 0 1.33 1.88 0.80 0.80 1.00 1.0
Metal2 10 0 1.88 2.33 0.80 0.80 0.85 1.0
Via2 29 0 2.33 2.88 1.00 0.22 0.21 1.0
Metal3 30 0 2.88 3.33 0.85 0.00 0.00 1.0
Via3 49 0 3.33 3.88 0.61 0.66 0.25 1.0
Metal4 50 0 3.88 4.33 0.58 0.91 0.22 1.0
Via4 66 0 4.33 4.88 0.87 0.67 0.37 1.0
Metal5 67 0 4.88 5.33 0.86 0.82 0.27 1.0
TopVia1 125 0 5.33 6.16 1.00 0.90 0.75 1.0
TopMetal1 126 0 6.16 8.16 1.00 0.90 0.75 1.0
TopVia2 133 0 8.16 11.16 1.00 0.50 0.00 1.0
TopMetal2 134 0 11.16 14.16 1.00 0.50 0.00 1.0
MIM 36 0 5.30 5.45 0.15 0.55 0.42 1.0
jakobsen@t14:~/opentools/GDS2glTF_fork/layerstack$
```

OpenROAD


OpenROAD
File View Tools Windows Options Help
Fit Find Congestion Setup Inspect Timing
0 10 20μm
Timing Report
Paths: 100 Update
Setup Hold
Capture Clock | Required | Arrival | Slack | Start | End
clk_in | -0.017 | 0.244 | 0.262 | spdif/_703_/Q | spdif/_704_/D
clk_in | -0.017 | 0.264 | 0.282 | spdif/_640_/Q | spdif/_640_/D
clk_in | -0.017 | 0.266 | 0.283 | spdif/_664_/Q | spdif/_664_/D
clk_in | -0.018 | 0.265 | 0.284 | i2c/_200_/Q | i2c/_200_/D
Path Details
Find Pin or Net Path: 1 Expand clock
Data Capture
Pin | Time | Delay | Slew | Load
clk_in ↑ | 0.000 | 0.000 | 0.000 | 0.384
spdif/_640_/CLK (sky130_fd_sc_hd__dfxtp_1) ↑ | 0.000 | 0.000 | 0.001
Inspector Timing Report
Scripting
33.00 33.00 clock clk_in (rise edge)
0.00 33.00 clock network delay (propagated)
0.00 33.00 clock reconvergence pessimism
33.00 ^ ctrl/tim/_96_/CLK (sky130_fd_sc_hd__dfxtp_1)
-0.91 32.09 library setup time
32.09 data required time
32.09 data required time
-14.61 data arrival time
17.48 slack (MET)
>>> report_tns
tns 0.00
Idle
TCL commands
Selected/Highlighted Shapes Scripting
-51.49600, 73.87700

Analog open source tools

Do not copy the Cadence/Mentor model - 20 year old tools without innovation

Learn how to do modern programming to learn how to abstract or team up with someone

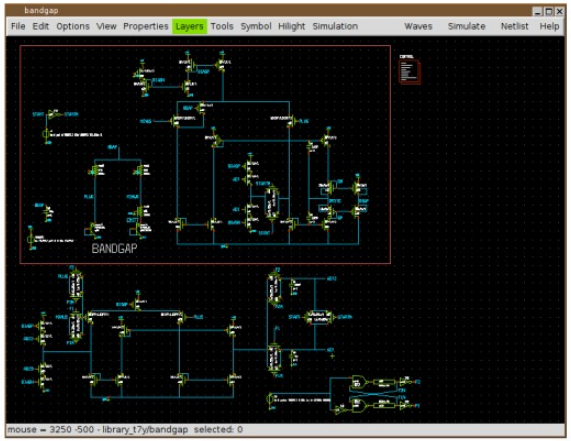
Build circuit and layout generators to do the job

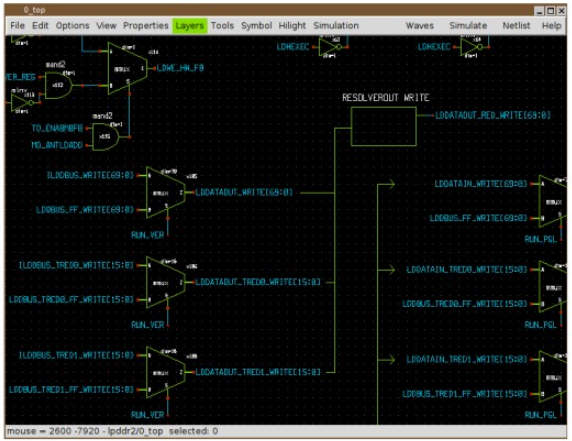
Lets check out https://github.com/mole99/tt08-aicd-playground

Analog Chip Design (front end)

Schematic editor

XSCHEM : schematic capture and netlisting EDA tool



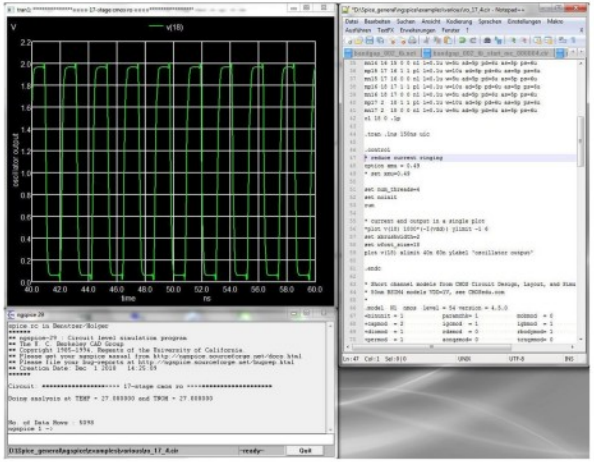


Analog circuit simulator

Xyce™ PARALLEL ELECTRONIC SIMULATOR

Parallel Spice simulator
From sandy National Laboratories

NGSPICE



Closer look at Xyce

On going development

Runs well on your laptop

And even faster on Allans servers

Heavy parallel codebase

Not limited by number of licenses



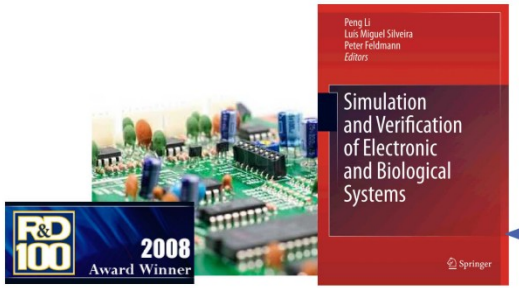
The Xyce Analog Circuit Simulator

- SPICE-Compatible syntax (Berkeley 3f5)
- Not “Fast SPICE”
- Two versions, **Serial** and…
- **Distributed Memory Parallel** (MPI-based)
- Unique solver algorithms
- Industry standard models
- Non-traditional models
  - Neuron/synapse
  - TCAD (PDE-based)

- http://xyce.sandia.gov

Open Source, GPLv3
- Since September of 2013 (Xyce 6.0)

Xyce Release 6.10
- November, 2018; 23rd major release
- >3,900 external downloads



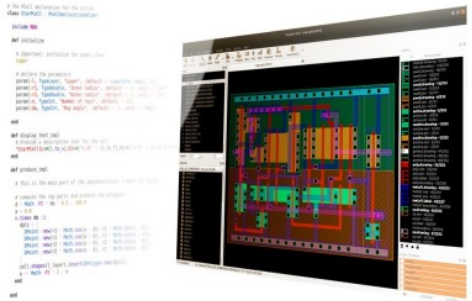
'DISTRIBUTION STATEMENT A. Approved for public release: distribution is unlimited. Approval ID: XXABW-2018-XXXX

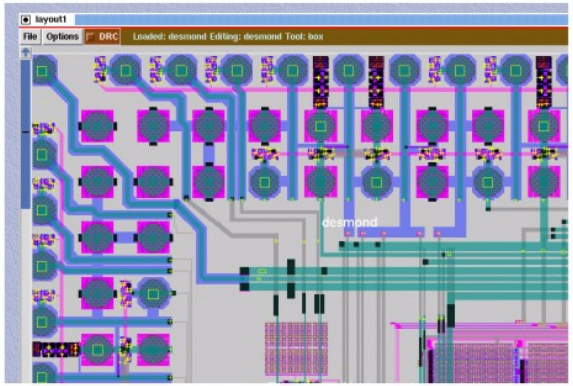
https://www.osti.gov/servlets/purl/1639584

Analog Layout

Magic VLSI Layout Tool

Current distribution version 8.2



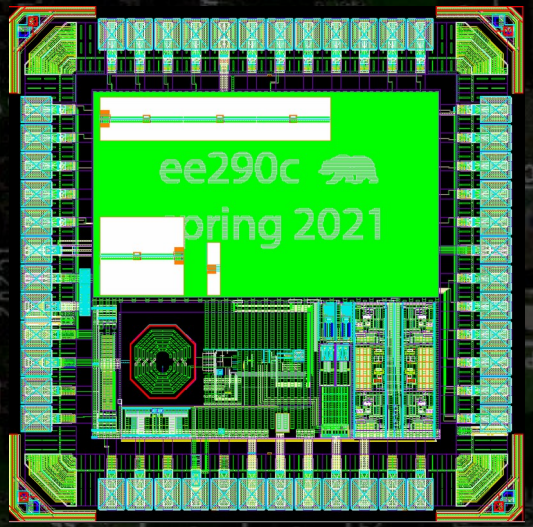


KLayout About Get KLayout Package Index Forum FSi

New ways to teach and learn Chip design

Berkeley engineering students pull off novel chip design in a single semester

Class shows successful model for expanding entry into field of semiconductor design



Protobuffers, Python and Rust

To do analog circuits and layout

https://engineering.berkeley.edu/news/2021/06/berkeley-engineering-students-design-novel-chip-in-semester-long-course/

Links and call to action

Online course outlet from VLSI System Design vlsisystemdesign.com

Install the tools https://github.com/britovski/sky130_skel

Installsky130 PDK https://github.com/RTimothyEdwards/open_pdks

Chip eco-system in Denmark : chipdesign.dk

Get in contact with me: Linkedin - jkj@icworks.dk - +45 51947707